LECTURE NOTES

ON

POWER ELECTRONICS

III B. Tech I semester (JNTUH-R13)

ELECTRICAL AND ELECTRONICS ENGINEERING

Unit-I

Power Semi Conductor Devices & Commutation Circuits

INTRODUCTION TO POWER ELECTRONICS:

Power Electronics is a field which combines Power (electric power), Electronics and Control systems.

Power engineering deals with the static and rotating power equipment for the generation, transmission and distribution of electric power.

Electronics deals with the study of solid state semiconductor power devices and circuits for Power conversion to meet the desired control objectives (to control the output voltage and output power).

Power electronics may be defined as the subject of applications of solid state power semiconductor devices (Thyristors) for the control and conversion of electric power.

Power electronics deals with the study and design of Thyristorised power controllers for variety of application like Heat control, Light/Illumination control, Motor control - AC/DC motor drives used in industries, High voltage power supplies, Vehicle propulsion systems, High voltage direct current (HVDC) transmission.

BRIEF HISTORY OF POWER ELECTRONICS

The first Power Electronic Device developed was the Mercury Arc Rectifier during the year 1900. Then the other Power devices like metal tank rectifier, grid controlled vacuum tube rectifier, ignitron, phanotron, thyratron and magnetic amplifier, were developed & used gradually for power control applications until 1950.

The first SCR (silicon controlled rectifier) or Thyristor was invented and developed by Bell Lab's in 1956 which was the first PNPN triggering transistor.

The second electronic revolution began in the year 1958 with the development of the commercial grade Thyristor by the General Electric Company (GE). Thus the new era of power electronics was born. After that many different types of power semiconductor devices & power conversion techniques have been introduced.The power electronics revolution is giving us the ability to convert, shape and control large amounts of power.

SOME APPLICATIONS OF POWER ELECTRONICS

Advertising, air conditioning, aircraft power supplies, alarms, appliances - (domestic and industrial), audio amplifiers, battery chargers, blenders, blowers, boilers, burglar alarms, cement kiln, chemical processing, clothes dryers, computers, conveyors, cranes and hoists, dimmers (light dimmers), displays, electric door openers, electric dryers, electric fans, electric vehicles, electromagnets, electro mechanical electro plating, electronic ignition, electrostatic precipitators, elevators, fans, flashers, food mixers, food warmer trays, fork lift trucks, furnaces, games, garage door openers, gas turbine starting, generator exciters, grinders, hand power tools, heat controls, high frequency lighting, HVDC transmission, induction heating, laser power supplies, latching relays, light flashers, linear induction motor controls, locomotives, machine tools, magnetic recording, magnets, mass transit railway system, mercury arc lamp ballasts, mining, model trains, motor controls, motor drives, movie projectors, nuclear reactor control rod, oil well drilling, oven controls, paper mills, particle accelerators, phonographs, photo copiers, power suppliers, printing press, pumps and compressors, radar/sonar power supplies, refrigerators, regulators, RF amplifiers, security systems, servo systems, sewing machines, solar power supplies, solid-state contactors, solid-state relays, static circuit breakers, static relays, steel mills, synchronous motor starting, TV circuits, temperature controls, timers and toys, traffic signal controls, trains, TV deflection circuits, ultrasonic generators, UPS, vacuum cleaners, VAR compensation, vending machines, VLF

transmitters, voltage regulators, washing machines, welding equipment.

POWER ELECTRONIC APPLICATIONS

COMMERCIAL APPLICATIONS

Heating Systems Ventilating, Air Conditioners, Central Refrigeration, Lighting, Computers and Office equipments, Uninterruptible Power Supplies (UPS), Elevators, and Emergency Lamps

DOMESTIC APPLICATIONS

Cooking Equipments, Lighting, Heating, Air Conditioners, Refrigerators & Freezers, Personal Computers, Entertainment Equipments, UPS.

INDUSTRIAL APPLICATIONS

Pumps, compressors, blowers and fans Machine tools, arc furnaces, induction furnaces, lighting control circuits, industrial lasers, induction heating, welding equipments

AEROSPACE APPLICATIONS

Space shuttle power supply systems, satellite power systems, aircraft power systems.

TELECOMMUNICATIONS

Battery chargers, power supplies (DC and UPS), mobile cell phone battery chargers

TRANSPORTATION

Traction control of electric vehicles, battery chargers for electric vehicles, electric locomotives, street cars, trolley buses, automobile electronics including engine controls

UTILITY SYSTEMS

High voltage DC transmission (HVDC), static VAR compensation (SVC), Alternative energy sources (wind, photovoltaic), fuel cells, energy storage systems, induced draft fans and boiler feed water pumps.

POWER SEMICONDUCTOR DEVICES

- Power Diodes.
- Power transistors (BJT's).
- Power MOSFETS.
- IGBT's.
- Thyristors

Thyristors are a family of p-n-p-n structured power semiconductor switching devices

SCR's (Silicon Controlled Rectifier)

The silicon controlled rectifier is the most commonly and widely used member of the thyristor family. The family of thyristor devices include SCR's, Diacs, Triacs, SCS, SUS, LASCR's and so on.

POWER SEMICONDUCTOR DEVICES USED IN POWER ELECTRONICS

The first thyristor or the SCR was developed in 1957. The conventional Thyristors (SCR's) were exclusively used for power control in industrial applications until 1970. After 1970, various types of power semiconductor devices were developed and became commercially available. The power semiconductor devices can be divided broadly into five types

- Power
- Diodes.
- Thyristors.
- Power BJT's.
- Power MOSFET's.
- Insulated Gate Bipolar Transistors (IGBT's).
  Static Induction Transistors (SIT's).

The Thyristors can be subdivided into different types

- Forced-commutated Thyristors (Inverter grade
- Thyristors) Line-commutated Thyristors (converter-grade
- Thyristors) Gate-turn off Thyristors (GTO).
- Reverse conducting Thyristors (RCT's).
- Static Induction Thyristors (SITH).
- Gate assisted turn-off Thyristors (GATT).
- Light activated silicon controlled rectifier (LASCR) or Photo
- SCR's. MOS-Controlled Thyristors (MCT's).

POWER DIODES

Power diodes are made of silicon p-n junction with two terminals, anode and cathode. P-N junction is formed by alloying, diffusion and epitaxial growth. Modern techniques in diffusion and epitaxial processes permit desired device characteristics.

The diodes have the following advantages

- High mechanical and thermal reliability
- High peak inverse voltage
- Low reverse current
- Low forward voltage drop
- High efficiency
- Compactness.

POWER TRANSISTORS

Power transistors are devices that have controlled turn-on and turn-off characteristics. These devices are used a switching devices and are operated in the saturation region resulting in low on-state voltage drop. They are turned on when a current signal is given to base or control terminal. The transistor remains on so long as the control signal is present. The switching speed of modern transistors is much higher than that of thyristors and are used extensively in dc-dc and dc-ac converters. However their voltage and current ratings are lower than those of thyristors and are therefore used in low to medium power applications.

Power transistors are classified as follows

- Bipolar junction transistors(BJTs)
- Metal-oxide semiconductor filed-effect transistors(MOSFETs)
- Static Induction transistors(SITs)
- Insulated-gate bipolar transistors(IGBTs)

BIPOLAR JUNCTION TRANSISTORS

The need for a large blocking voltage in the off state and a high current carrying capability in the on state means that a power BJT must have substantially different structure than its small signal equivalent. The modified structure leads to significant differences in the I-V characteristics and switching behavior between power transistors and its logic level counterpart.

POWER TRANSISTOR STRUCTURE

If we recall the structure of conventional transistor we see a thin p-layer is sandwiched between two n-layers or vice versa to form a three terminal device with the terminals named as Emitter, Base and Collector.

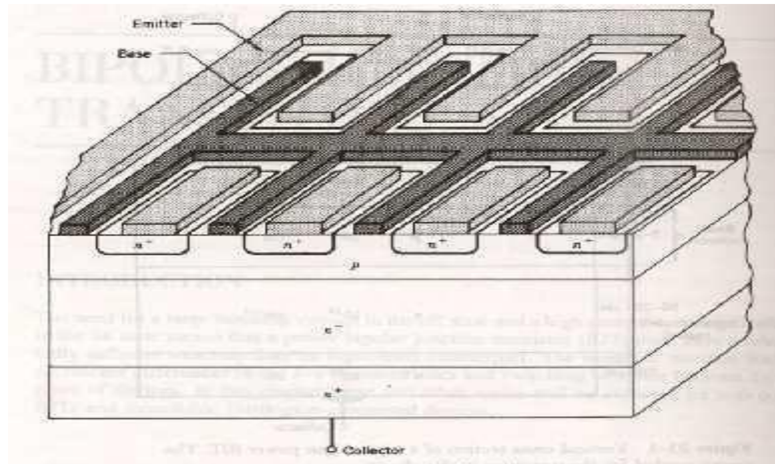
The difference in the two structures is obvious.

A power transistor is a vertically oriented four layer structure of alternating p-type and n-type. The vertical structure is preferred because it maximizes the cross sectional area and through which the current in the device is flowing. This also minimizes on-state resistance and thus power dissipation in the transistor.

The doping of emitter layer and collector layer is quite large typically 10^{19} cm^{-3}. A special layer called the collector drift region (n^-) has a light doping level of 10^{14}.

The thickness of the drift region determines the breakdown voltage of the transistor. The base thickness is made as small as possible in order to have good amplification capabilities, however if the base thickness is small the breakdown voltage capability of the transistor is compromised.

Practical power transistors have their emitters and bases interleaved as narrow fingers as shown. The purpose of this arrangement is to reduce the effects of current crowding. This multiple emitter layout also reduces parasitic ohmic resistance in the base current path which reduces power dissipation in the transistor.



STEADY STATE CHARACTERISTICS

Figure 3(a) shows the circuit to obtain the steady state characteristics. Fig 3(b) shows the input characteristics of the transistor which is a plot of I_B versus V_{BE} . Fig 3(c) shows the output characteristics of the transistor which is a plot I_C versus V_{CE} . The characteristics shown are that for a signal level transistor.

The power transistor has steady state characteristics almost similar to signal level transistors except that the V-I characteristics has a region of quasi saturation as shown by figure 4.

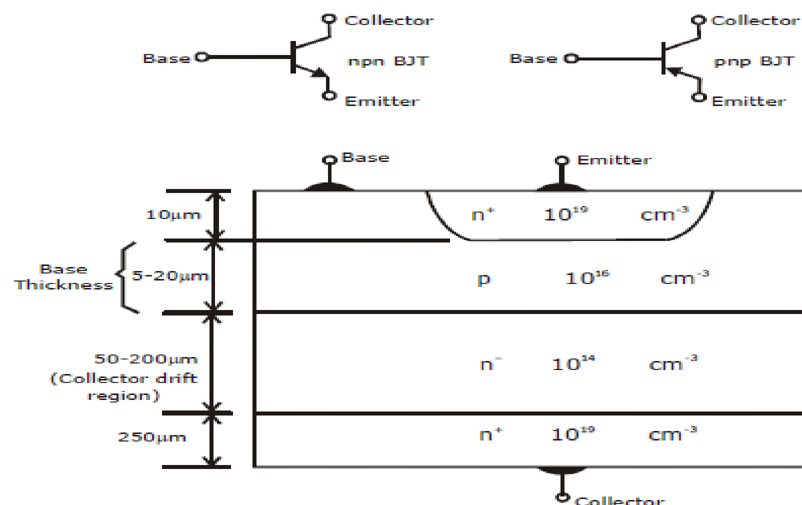
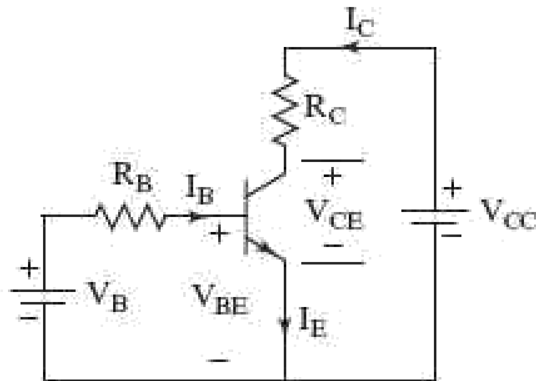
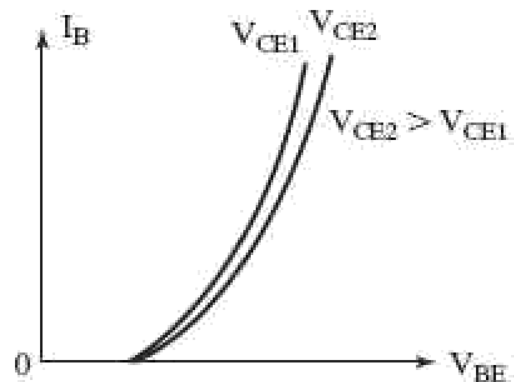


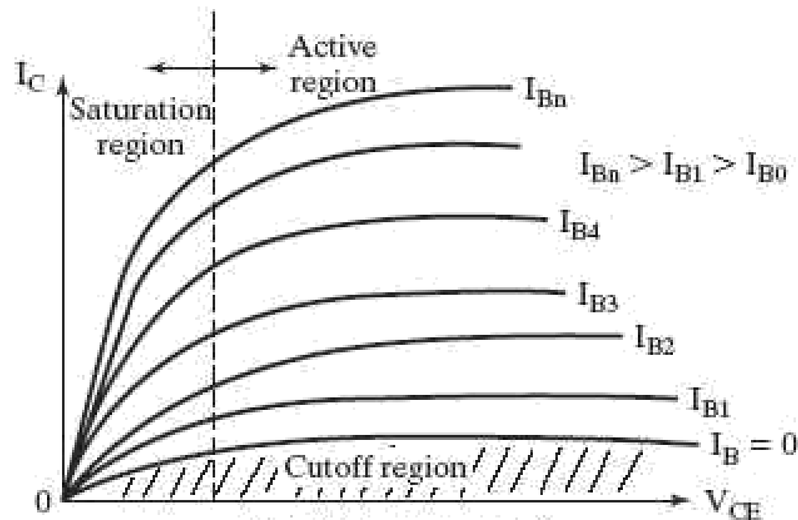
Fig. 1: Structure of Power Transistor



(a) Circuit diagram



(b) Input characteristics



(c) Output characteristics

There are four regions clearly shown: Cutoff region, Active region, quasi saturation and hard saturation. The cutoff region is the area where base current is almost zero. Hence no collector current flows and transistor is off. In the quasi saturation and hard saturation, the base drive is applied and transistor is said to be on. Hence collector current flows depending upon the load. The power BJT is never operated in the active region (i.e. as an amplifier) it is always operated between cutoff and saturation. The BV_{SUS} is the maximum collector to emitter voltage that can be sustained when BJT is carrying substantial collector current. The BV_{CEO} is the maximum collector to emitter breakdown voltage that can be sustained when base current is zero and BV_{CBO} is the collector base breakdown voltage when the emitter is open circuited

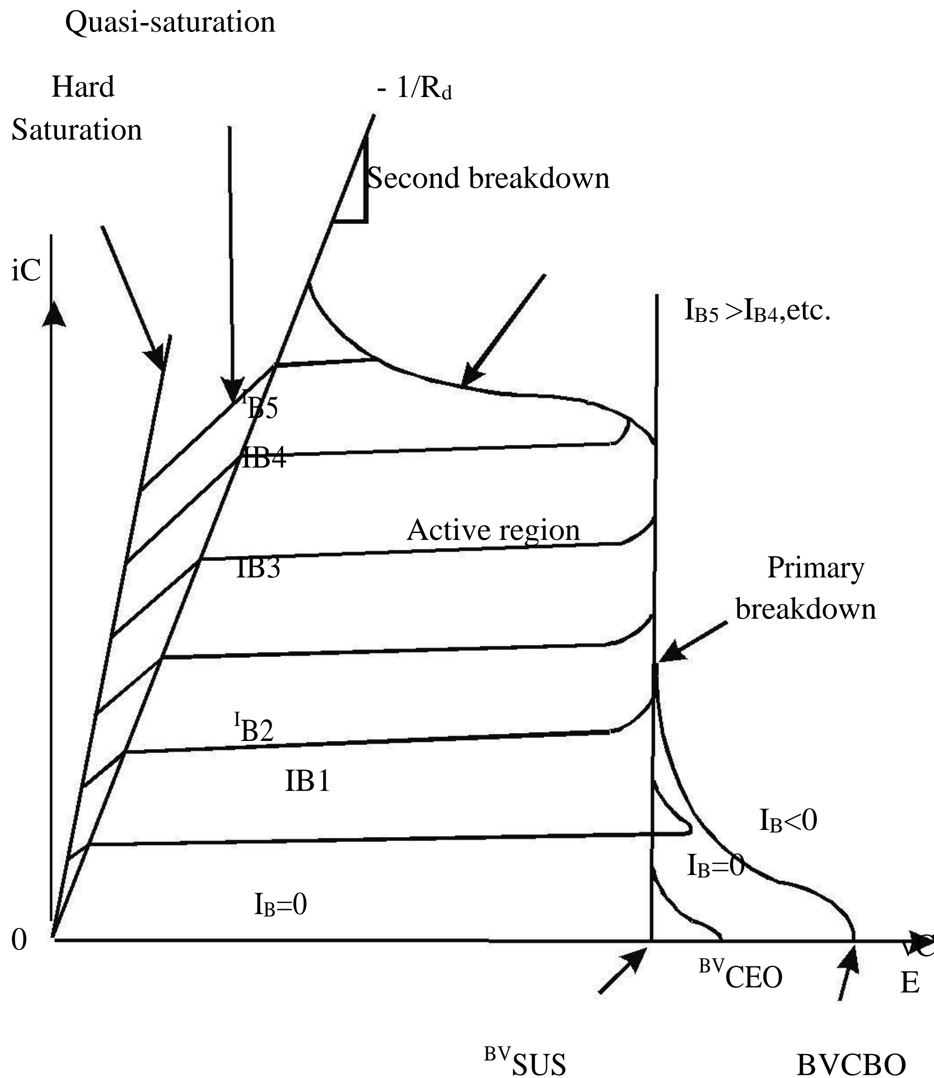


Fig. 4: Characteristics of NPN Power Transistors

The primary breakdown shown takes place because of avalanche breakdown of collector base junction. Large power dissipation normally leads to primary breakdown.

The second breakdown shown is due to localized thermal runaway. This is explained in detail later.

TRANSFER CHARACTERISTICS

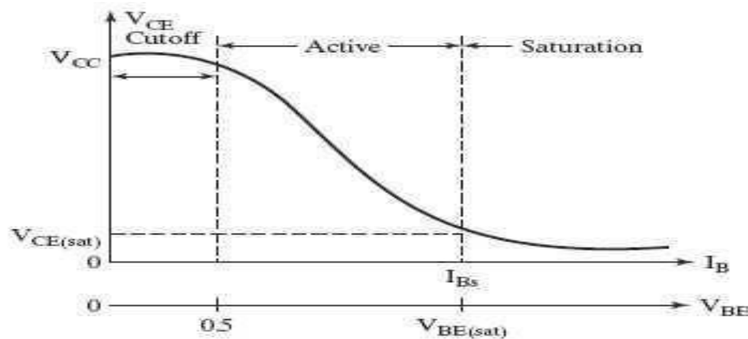


Fig. 5: Transfer Characteristics

TRANSISTOR AS A SWITCH

The transistor is used as a switch therefore it is used only between saturation and cutoff. From fig. 5 we can write the following equations

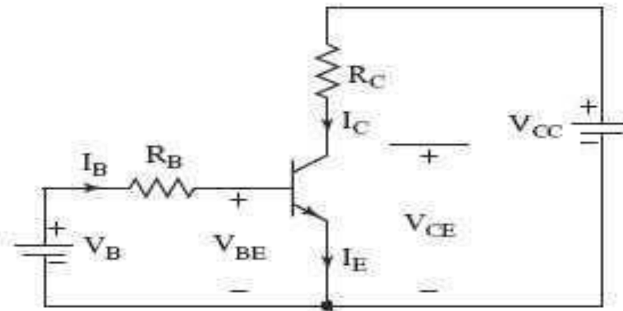


Fig. 6: Transistor Switch

If the base current is increased above I_{BM} ,V_{BE} increases, the collector current increases and V_{CE} falls belowV_{BE} . This continues until the CBJ is forward biased with V_{BC} of about 0.4 to 0.5V, the transistor than goes into saturation. The transistor saturation may be defined as the point above which any increase in the base current does not increase the collector current significantly.

In saturation, the collector current remains almost constant. If the collector emitter voltage is $V_{CE\,sat}$ the collector current is

V_{BE} increases due to increased base current resulting in increased power loss. Once the transistor is saturated, the CE voltage is not reduced in relation to increase in base current. However the power is increased at a high value of ODF, the transistor may be damaged due to thermal runaway. On the other hand if the transistor is under driven. I_B □ I_{BS} it may operate in active region, V_{CE} increases resulting in increased power loss.

SWITCHING CHARACTERISTICS

A forward biased p-n junction exhibits two parallel capacitances; a depletion layer capacitance and a diffusion capacitance. On the other hand, a reverse biased p-n junction has only depletion capacitance. Under steady state the capacitances do not play any role. However under transient conditions, they influence turn-on and turn-off behavior of the transistor.

TRANSIENT MODEL OF BJT

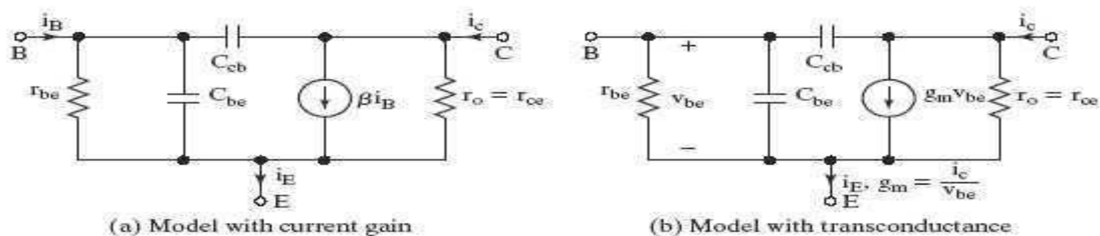


Fig. 7: Transient Model of BJT

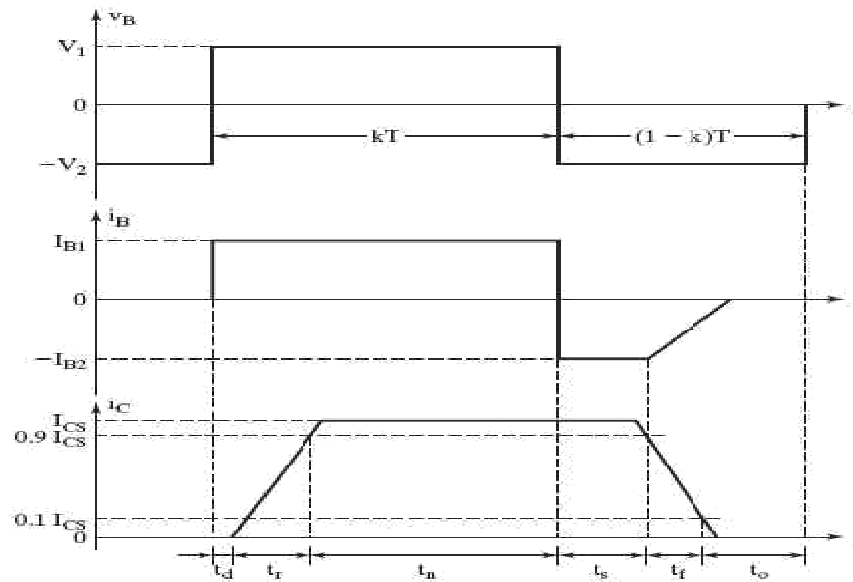


Fig. 8: Switching Times of BJT

Due to internal capacitances, the transistor does not turn on instantly. As the voltage V_B rises from zero to V_1 and the base current rises to I_{B1}, the collector current does not respond immediately. There is a delay known as delay time td, before any collector current flows. The delay is due to the time required to charge up the BEJ to the forward bias voltage V_{BE}(0.7V). The collector current rises to the steady value of I_{CS} and this time is called rise time t_r.

The base current is normally more than that required to saturate the transistor. As a result excess minority carrier charge is stored in the base region. The higher the ODF, the greater is the amount of extra charge stored in the base. This extra charge which is called the saturating charge is proportional to the excess base drive.

This extra charge which is called the saturating charge, is proportional to the excess base drive and the corresponding current I_e.

When the input voltage is reversed from V_1 to $-V_2$, the reverse current $–I_{B2}$ helps to discharge the base. Without $–I_{B2}$ the saturating charge has to be removed entirely due to recombination and the storage time t_s would be longer.

Once the extra charge is removed, BEJ charges to the input voltage $–V_2$ and the base current falls to zero. t_f depends on the time constant which is determined by the reverse biased BEJ capacitance.

Turn-on time t_{on} **:** The turn-on time can be decreased by increasing the base drive for a fixed value of collector current. t_d is dependent on input capacitance does not change significantly with I_C . However t_r increases with increase in I_C .

Turn off time t_{off} : The storage time is dependent on over drive factor and does not change significantly with I_C. t_f is function of capacitance and increases with I_C. t_s & t_f can be reduced by providing negative base drive during turn-off. t_f is less sensitive to negative base drive.

Cross-over t_C **:** The crossover time t_C is defined as the interval during which the collector voltage V_{CE} rises from 10% of its peak off state value and collector current. I_C falls to

10% of its on-state value. t_C is a function of collector current negative base drive.

POWER DERATING

Fig. 11: Thermal Equivalent Circuit of Transistor

BREAK DOWN VOLTAGES

A break down voltage is defined as the absolute maximum voltage between two terminals with the third terminal open, shorted or biased in either forward or reverse direction.

BV_{SUS} : The maximum voltage between the collector and emitter that can be sustained across the transistor when it is carrying substantial collector current.

BV_{CEO} **:** The maximum voltage between the collector and emitter terminal with base open circuited.

BV_{CBO} **:** This is the collector to base break down voltage when emitter is open circuited.

BASE DRIVE CONTROL

This is required to optimize the base drive of transistor. Optimization is required to increase switching speeds. t_{on} can be reduced by allowing base current peaking during can be increased to a sufficiently high value to maintain the transistor in quasi-saturation region. t_{off} can be reduced by reversing base current and allowing base current peaking during turn off since increasing I_{B2} decreases storage time.

A typical waveform for base current is shown.

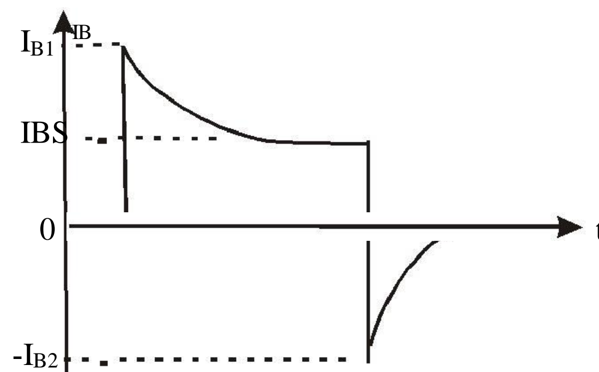


Fig. 12: Base Drive Current Waveform

Some common types of optimizing base drive of transistor are

Turn-on Control.

Turn-off Control.

Proportional Base Control.

Antisaturation Control

ADVANTAGES OF BJT'S

- BJT's have high switching frequencies since their turn-on and turn-off time are low.
- The turn-on losses of a BJT are small.
- BJT has controlled turn-on and turn-off characteristics since base drive control is possible.
- BJT does not require commutation circuits.

DEMERITS OF BJT

- Drive circuit of BJT is complex.
- It has the problem of charge storage which sets a limit on switching frequencies. It cannot be used in parallel operation due to problems of negative temperature coefficient.

POWER MOSFETS

INTRODUCTION TO FET'S

FET's use field effect for their operation. FET is manufactured by diffusing two areas of p-type into the n-type semiconductor as shown. Each p-region is connected to a gate terminal; the gate is a p-region while source and drain are n-region. Since it is similar to two diodes one is a gate source diode and the other is a gate drain diode.

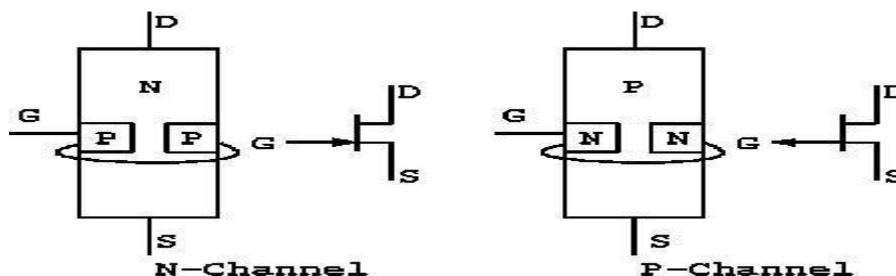


Fig:1: Schematic symbol of JFET

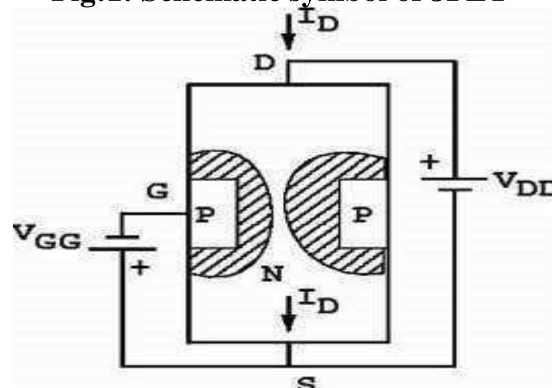


Fig. 2: Structure of FET with biasing

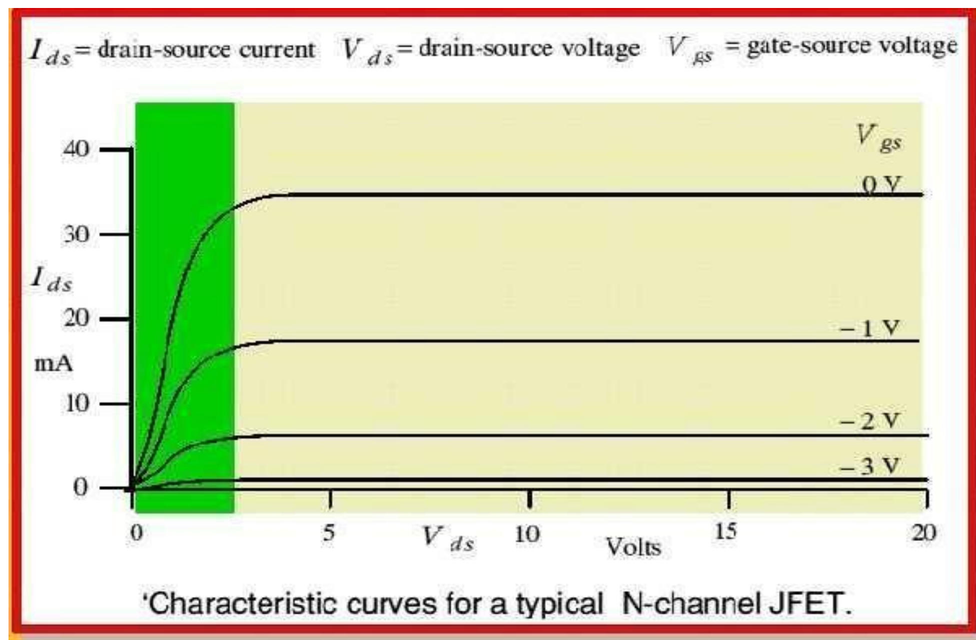
In BJT's we forward bias the B-E diode but in a JFET, we always reverse bias the gate-source diode. Since only a small reverse current can exist in the gate lead. Therefore I_G 0 , therefore R_{in} *ideal* .

The term field effect is related to the depletion layers around each p-region as shown. When the supply voltage *VDD* is applied as shown it forces free electrons to flow from source to drain. With gate reverse biased, the electrons need to flow from source to drain, they must pass through the narrow channel between the two depletion layers. The more the negative gate voltage is the tighter the channel becomes.

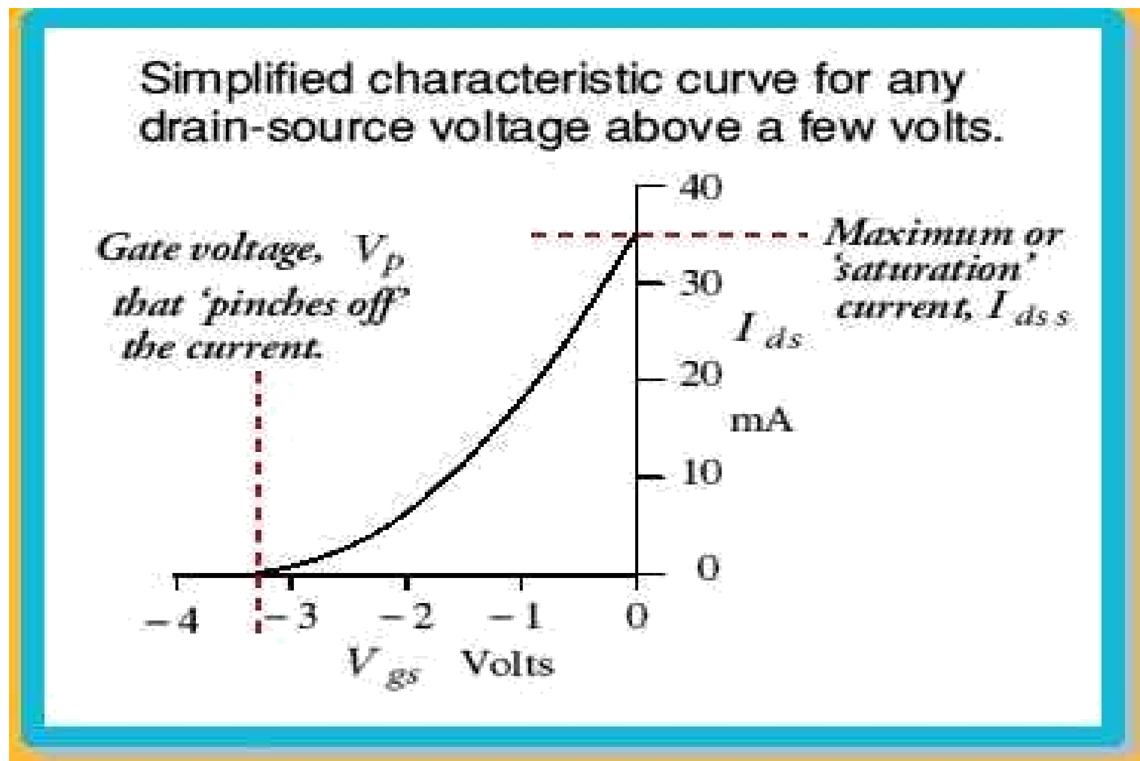
Therefore JFET acts as a voltage controlled device rather than a current controlled device.

JFET has almost infinite input impedance but the price paid for this is loss of control over the output current, since JFET is less sensitive to changes in the output voltage than a BJT.

JFET CHARACTERISTICS



'Characteristic curves for a typical N-channel JFET.



The maximum drain current out of a JFET occurs when V_{GS} V_{DS} is increased for 0 to a few volts, the current will increase as determined by ohms law. As V_{DS} approaches V_P the depletion region will widen, carrying a noticeable reduction in channel width. If V_{DS} is increased to a level where the two depletion region would touch a pinch-off will result. I_D now maintains a saturation level I_{DSS} . Between 0 volts and pinch off voltage V_P is the ohmic region. After V_P , the regions constant current or active region.

If negative voltage is applied between gate and source the depletion region similar to those obtained with V_{GS}=□ 0 are formed but at lower values of V_{DS} . Therefore saturation level is reached earlier.

Classification of MOSFET

MOSFET stands for metal oxide semiconductor field effect transistor. There are two types of MOSFET

- Depletion type MOSFET
- Enhancement type MOSFET

DEPLETION TYPE MOSFET

CONSTRUCTION

Symbol of n-channel depletion type MOSFET

It consists of a highly doped p-type substrate into which two blocks of heavily doped n-type material are diffused to form a source and drain. A n-channel is formed by diffusing between source and drain. A thin layer of SiO_2 is grown over the entire surface and holes are cut in SiO_2 to make contact with n-type blocks. The gate is also connected to a metal contact surface but remains insulated from the n-channel by the SiO_2 layer. SiO_2 layer results in an extremely high input impedance of the order of 10^{10} to 10^{15} Ω for this area.

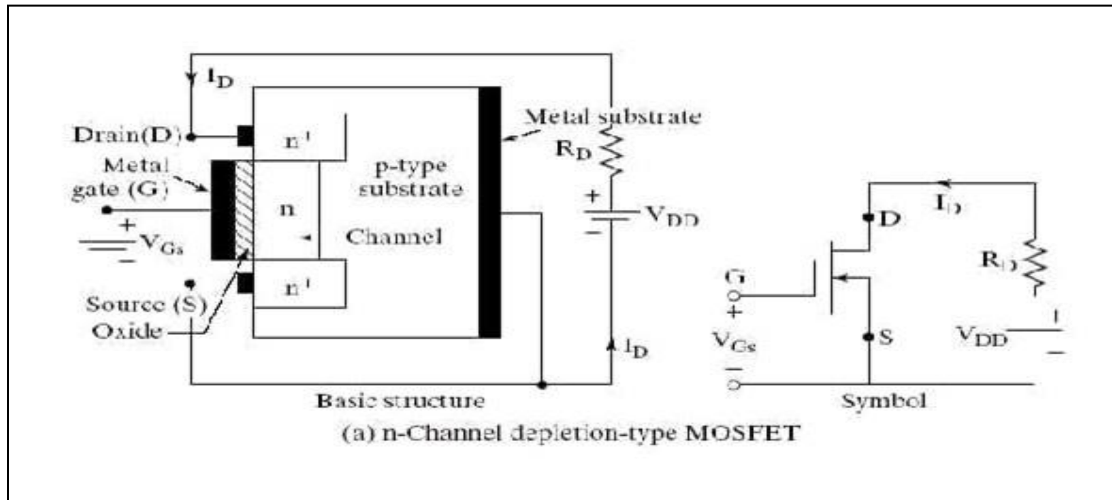


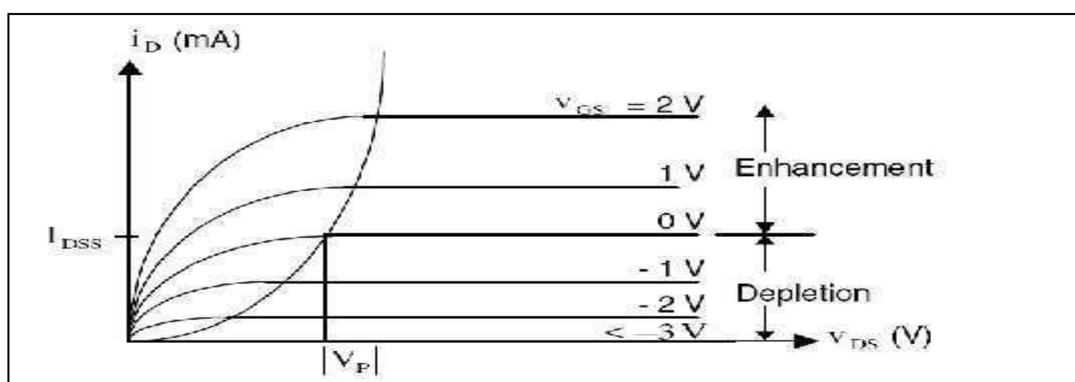
fig. 4: Structure of n-channel depletion type MOSFET

OPERATION

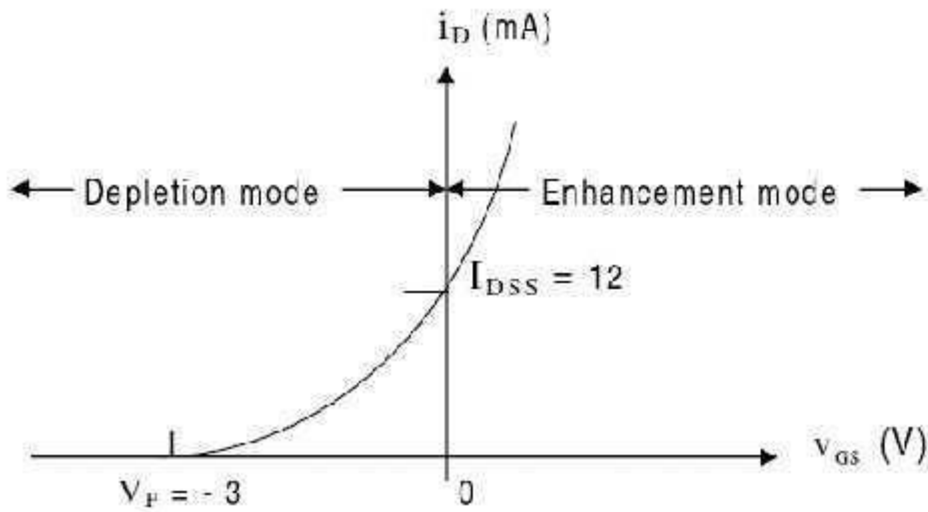
When $V_{GS} = 0V$ and V_{DS} is applied and current flows from drain to source similar to JFET. When $V_{GS} = -1V$, the negative potential will tend to pressure electrons towards the p-type substrate and attracts hole from p-type substrate. Therefore recombination occurs and will reduce the number of free electrons in the n-channel for conduction. Therefore with increased negative gate voltage I_D reduces.

For positive values, V_{gs}, additional electrons from p-substrate will flow into the channel and establish new carriers which will result in an increase in drain current with positive gate voltage.

DRAIN CHARACTERISTICS



TRANSFER CHARACTERISTICS



ENHANCEMENT TYPE MOSFET

Here current control in an n-channel device is now affected by positive gate to source voltage rather than the range of negative voltages of JFET's and depletion type MOSFET.

BASIC CONSTRUCTION

A slab of p-type material is formed and two n-regions are formed in the substrate. The source and drain terminals are connected through metallic contacts to n-doped regions, but the absence of a channel between the doped n-regions. The SiO_2 layer is still present to isolate the gate metallic platform from the region between drain and source, but now it is separated by a section of p-type material.

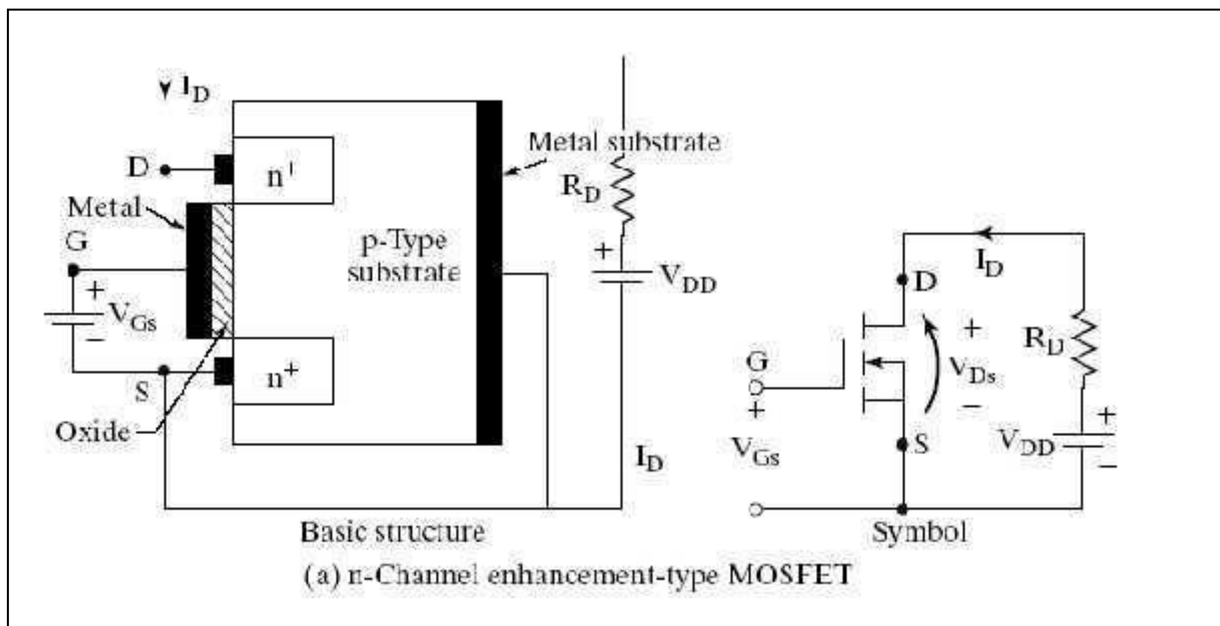


Fig. 5: Structure of n-channel enhancement type MOSFET

OPERATION

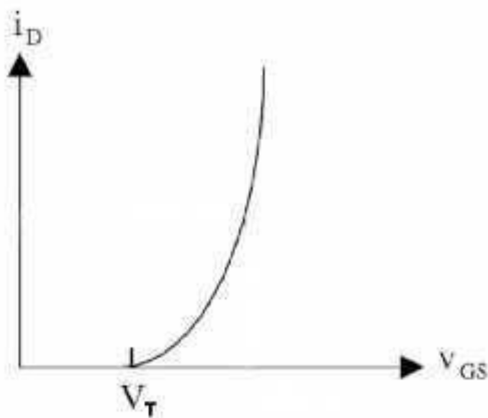
If V_{GS} □ $0V$ and a voltage is applied between the drain and source, the absence of a n-channel will result in a current of effectively zero amperes. With V_{DS} set at some positive voltage and V_{GS} set at 0V, there are two reverse biased p-n junctions between the n-doped regions and p substrate to oppose any significant flow between drain and source.

If both V_{DS} and V_{GS} have been set at some positive voltage, then positive potential at the gate will pressure the holes in the p-substrate along the edge of SiO_2 layer to leave the area and enter deeper region of p-substrate. However the electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The negative carriers will not be absorbed due to insulating SiO_2 layer, forming an inversion layer which results in current flow from drain to source.

The level of V_{GS} that results in significant increase in drain current is called threshold voltage V_T . As V_{GS} increases the density of free carriers will increase resulting in increased level of drain current. If V_{GS} is constant V_{DS} is increased; the drain current will eventually reach a saturation level as occurred in JFET.

DRAIN CHARACTERISTICS

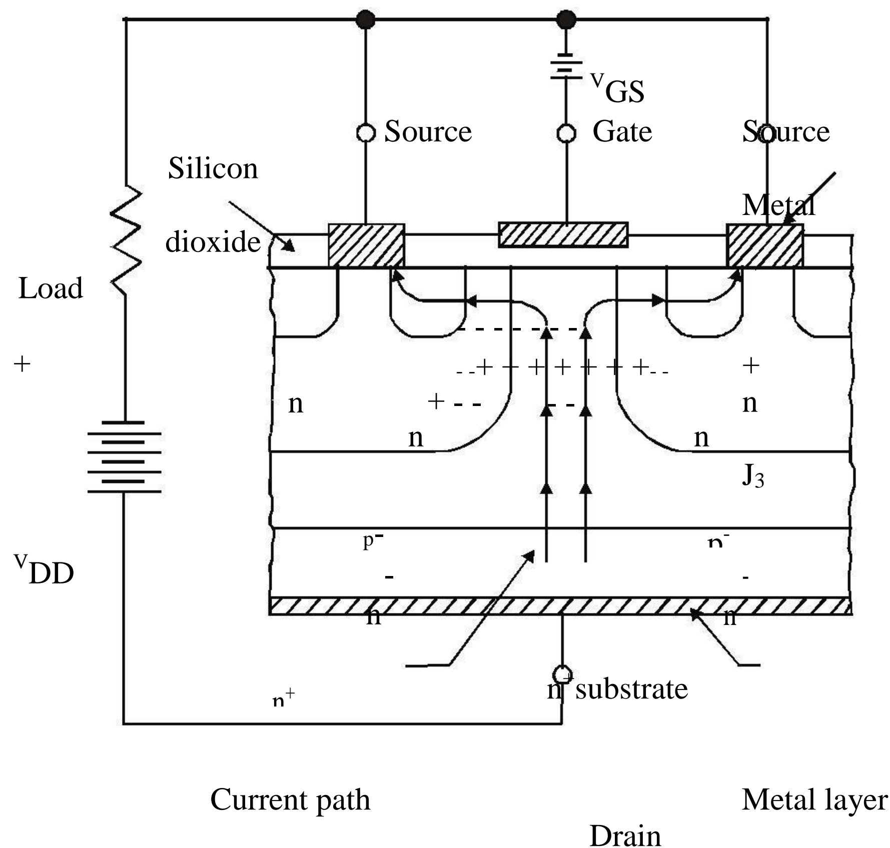
TRANSFER CHARACTERISTICS



POWER MOSFET'S

Power MOSFET's are generally of enhancement type only. This MOSFET is turned 'ON' when a voltage is applied between gate and source. The MOSFET can be turned 'OFF' by removing the gate to source voltage. Thus gate has control over the conduction of the MOSFET. The turn-on and turn-off times of MOSFET's are very small. Hence they operate at very high frequencies; hence MOSFET's are preferred in applications such as choppers and inverters. Since only voltage drive (gate-source) is required, the drive circuits of MOSFET are very simple. The paralleling of MOSFET's is easier due to their positive temperature coefficient. But MOSFTS's have high on-state resistance hence for higher currents; losses in the MOSFET's are substantially increased. Hence MOSFET's are used for low power applications.

CONSTRUCTION



determines the voltage blocking capability of the device. On the other side of *n* substrate, a metal layer is deposited to form the drain terminal. Now *p* regions are diffused in the epitaxially grown *n* layer. Further *n* regions are diffused in the *p* regions as shown.

SiO_2 layer is added, which is then etched so as to fit metallic source and gate terminals.

A power MOSFET actually consists of a parallel connection of thousands of basic MOSFET cells on the same single chip of silicon.

When gate circuit voltage is zero and V_{DD} is present, *n* *p* junctions are reverse biased and no current flows from drain to source. When gate terminal is made positive with respect to source, an electric field is established and electrons from *n* channel in the *p* regions. Therefore a current from drain to source is established.

Power MOSFET conduction is due to majority carriers therefore time delays caused by removal of recombination of minority carriers is removed.

Because of the drift region the ON state drop of MOSFET increases. The thickness of the drift region determines the breakdown voltage of MOSFET. As seen a parasitic BJT is formed, since emitter base is shorted to source it does not conduct.

SWITCHING CHARACTERISTICS

The switching model of MOSFET's is as shown in the figure 6(a). The various inter electrode capacitance of the MOSFET which cannot be ignored during high frequency switching are represented by C_{gs}, C_{gd} & C_{ds}. The switching waveforms are as shown in figure 7 . The turn on time t_d is the time that is required to charge the input capacitance to the threshold voltage level. The rise time t_r is the gate charging time from this threshold level to the full gate voltage V_{gsp} . The turn off delay time t_{doff} is the time required for the input capacitance to discharge from overdriving the voltage V_1 to the pinch off region. The fall time is the time required for the input capacitance to discharge from pinch off region to the threshold voltage. Thus basically switching ON and OFF depend on the charging time of the input gate capacitance.

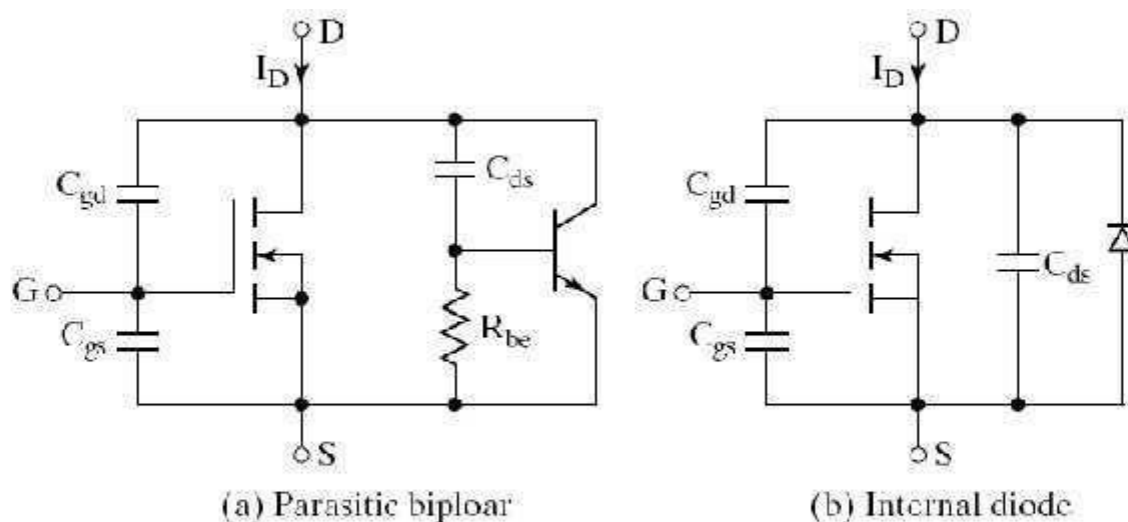
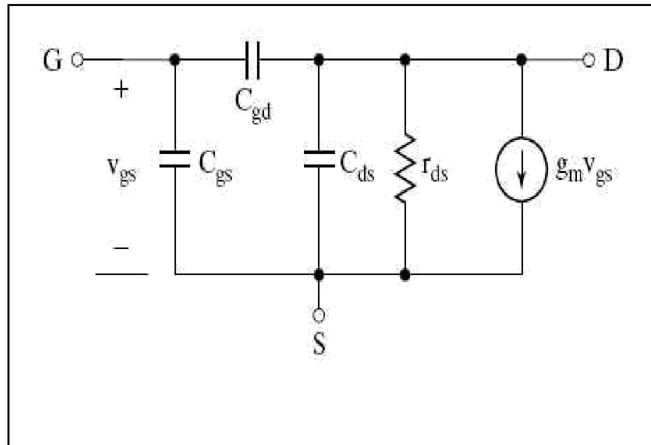


Fig.6: Switching model of MOSFET



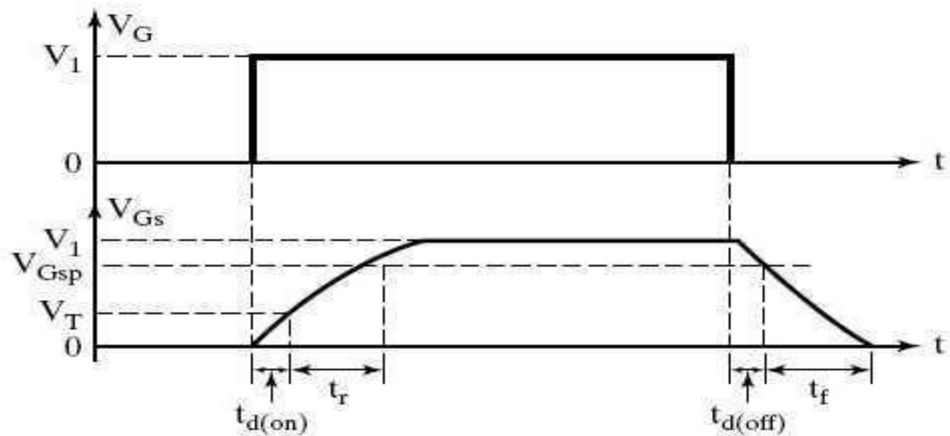


Fig.7: Switching waveforms and times of Power MOSFET

GATE DRIVE

The turn-on time can be reduced by connecting a RC circuit as shown to charge the capacitance faster. When the gate voltage is turned on, the initial charging current of the capacitance is

Where R_S is the internal resistance of gate drive force

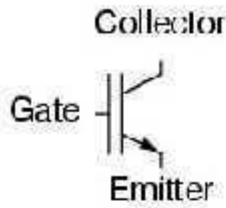
COMPARISON OF MOSFET WITH BJT

- Power MOSFETS have lower switching losses but its on-resistance and conduction losses are more. A BJT has higher switching loss bit lower conduction loss. So at high frequency applications power MOSFET is the obvious choice. But at lower operating frequencies BJT is superior.
- MOSFET has positive temperature coefficient for resistance. This makes parallel operation of MOSFET's easy. If a MOSFET shares increased current initially, it heats up faster, its resistance increases and this increased resistance causes this current to shift to other devices in parallel. A BJT is a negative temperature coefficient, so current shaving resistors are necessary during parallel operation of BJT's.
- In MOSFET secondary breakdown does not occur because it have positive temperature coefficient. But BJT exhibits negative temperature coefficient which results in secondary breakdown.

  Power MOSFET's in higher voltage ratings have more conduction losses.

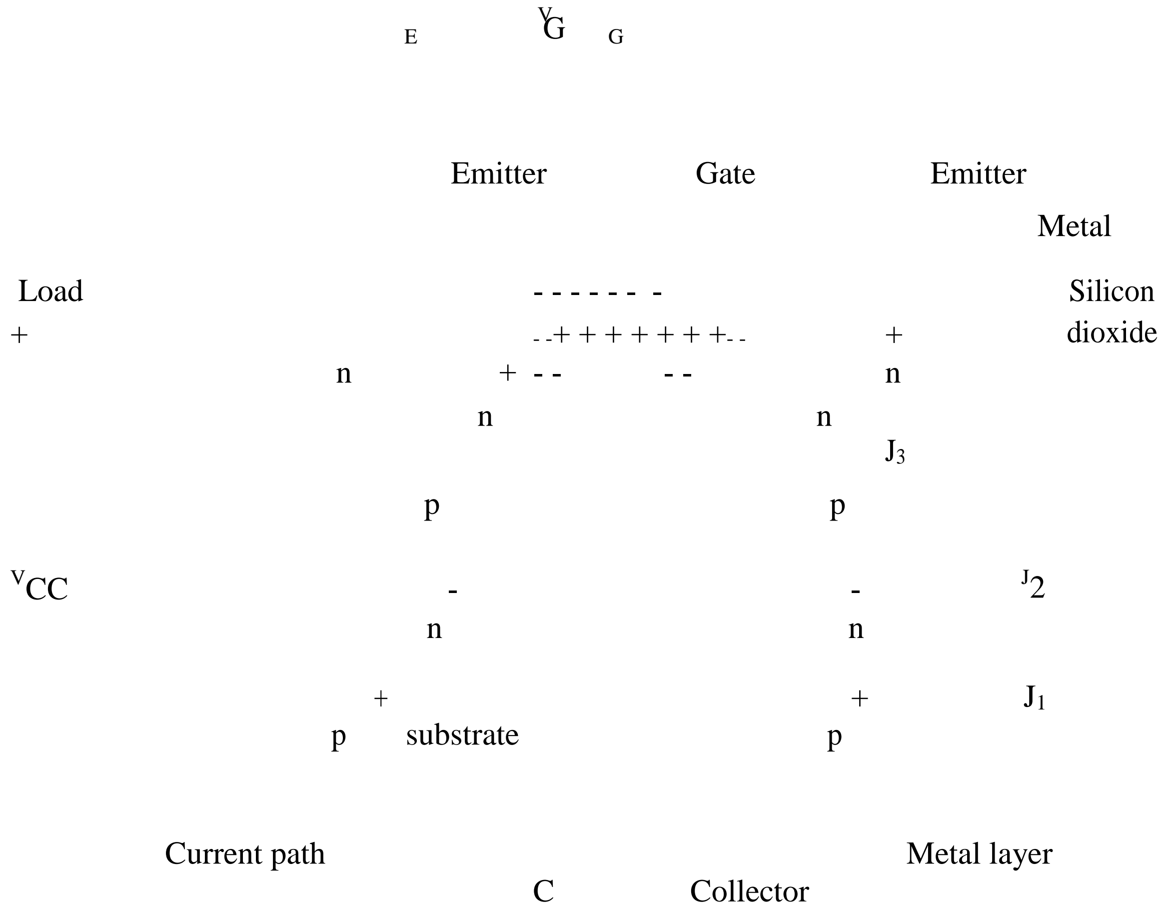
  Power MOSFET's have lower ratings compared to BJT's . Power MOSFET's □ 500V to 140A, BJT □ 1200V, 800A.

1.23. MOSIGT OR IGBT



The metal oxide semiconductor insulated gate transistor or IGBT combines the advantages of BJT's and MOSFET's.
Therefore an IGBT has high input impedance like a MOSFET and low-on state power loss as in a BJT. Further IGBT is free from second breakdown problem present in BJT.

1.23.1 IGBT BASIC STRUCTURE AND WORKING



It is constructed virtually in the same manner as a power MOSFET. However, the substrate is now a *p* layer called the collector.

When gate is positive with respect to positive with respect to emitter and with gate emitter voltage greater than V_{GSTH}, an n channel is formed as in case of power MOSFET. This *n* channel short circuits the *n* region with *n* emitter regions.

An electron movement in the *n* channel in turn causes substantial hole injection from *p* substrate layer into the epitaxially *n* layer. Eventually a forward current is established.

MOSFET is formed with input gate, emitter as source and *n* region as drain. Equivalent circuit is as shown below.

Also *p* serves as collector for pnp device and also as base for npn transistor. The two pnp and npn is formed as shown.

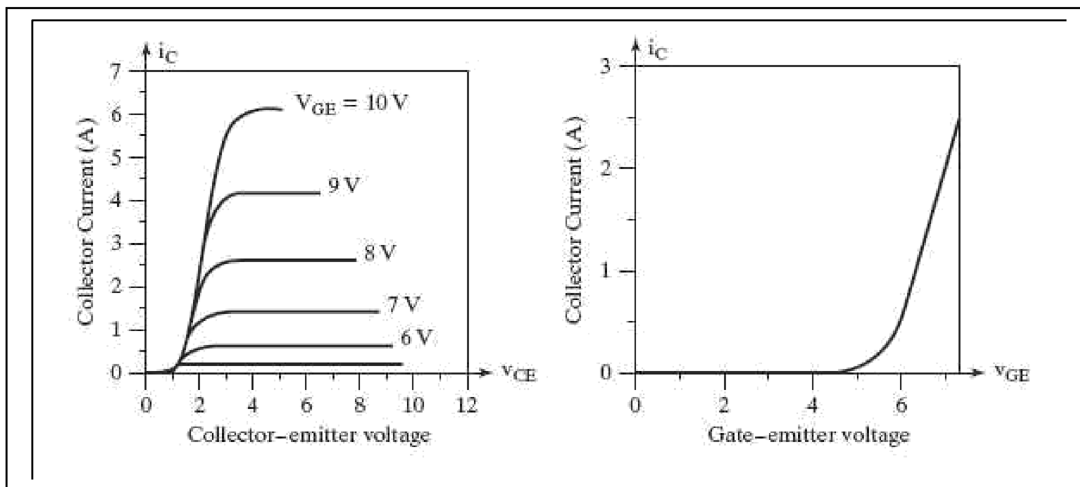
V_{GS} V_{GSth} T_1

Therefore T_1 starts conducting. The collector of T_1 is base of T_2 . Therefore regenerative action takes place and large number of carriers are injected into the *n* drift region. This reduces the ON-state loss of IGBT just like BJT.

When gate drive is removed IGBT is turn-off. When gate is removed the induced channel will vanish and internal MOSFET will turn-off. Therefore T_1 will turn-off it T_2 turns off.

Structure of IGBT is such that R_1 is very small. If R_1 small T_1 will not conduct therefore IGBT's are different from MOSFET's since resistance of drift region reduces when gate drive is applied due to *p* injecting region. Therefore ON state IGBT is very small.

IGBT CHARACTERISTICS



STATIC CHARACTERISTICS

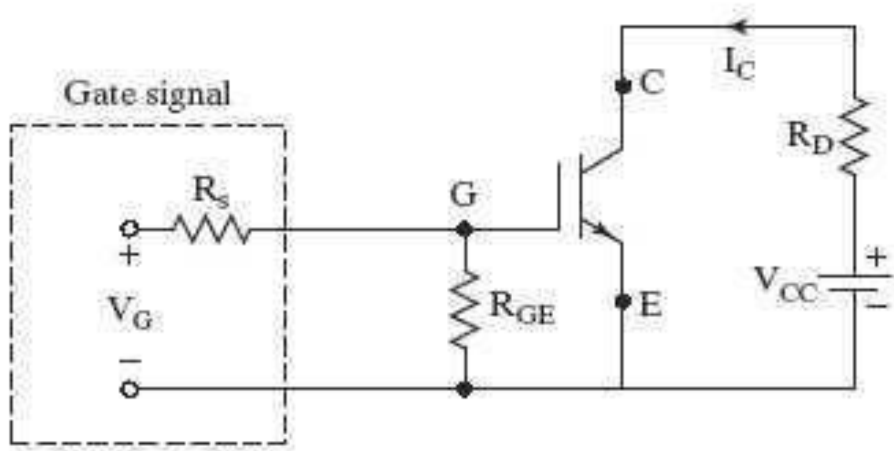


Fig. 9: IGBT bias circuit

Static V-I characteristics (I_C versus V_{CE})

Same as in BJT except control is by V_{GE} . Therefore IGBT is a voltage controlled device.

Transfer Characteristics (I_C versus V_{GE})

Identical to that of MOSFET. When V_{GE} V_{GET} , IGBT is in off-state.

APPLICATIONS

Widely used in medium power applications such as DC and AC motor drives, UPS systems, Power supplies for solenoids, relays and contractors.

Though IGBT's are more expensive than BJT's, they have lower gate drive requirements, lower switching losses. The ratings up to 1200V, 500A.

SERIES AND PARALLEL OPERATION

Transistors may be operated in series to increase their voltage handling capability. It is very important that the series-connected transistors are turned on and off simultaneously. Other wise, the slowest device at turn-on and the fastest devices at turn-off will be subjected to the full voltage of the collector emitter circuit and the particular device may be destroyed due to high voltage. The devices should be matched for gain, transconductance, threshold voltage, on state voltage, turn-on time, and turn-off time. Even the gate or base drive characteristics should be identical.

Transistors are connected in parallel if one device cannot handle the load current demand. For equal current sharings, the transistors should be matched for gain, transconductance, saturation voltage, and turn-on time and turn-off time. But in practice, it is not always possible to meet these requirements. A reasonable amount of current sharing (45 to 55% with two transistors) can be obtained by connecting resistors in series with the emitter terminals as shown in the figure 10.

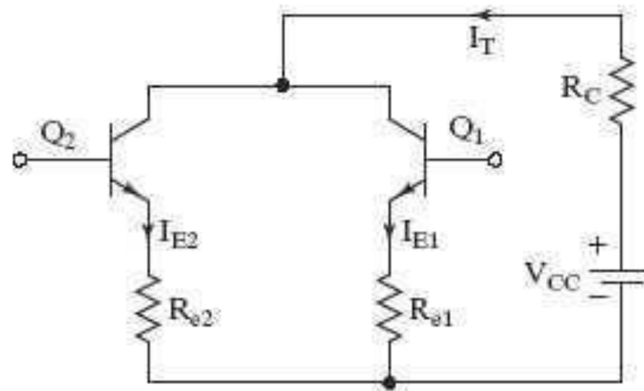


Fig. 10: Parallel connection of Transistors

The resistor will help current sharing under steady state conditions. Current sharing under dynamic conditions can be accomplished by connecting coupled inductors. If the current through Q_1 rises, the $l\,di/dt$ across L_1 increases, and a corresponding voltage of opposite polarity is induced across inductor L_2 . The result is low impedance path, and the current is shifted to Q_2 . The inductors would generate voltage spikes and they may be expensive and bulky, especially at high currents.

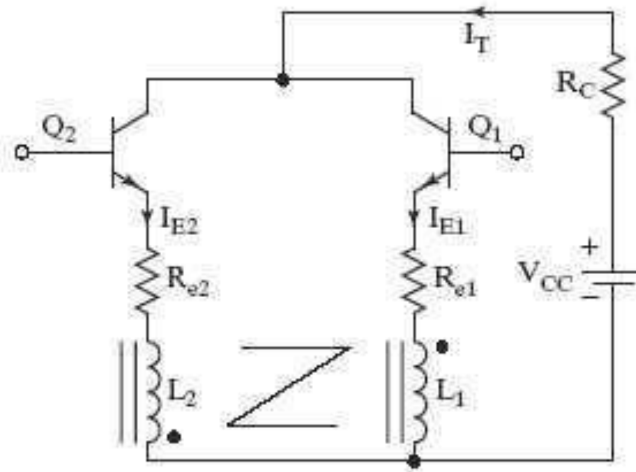
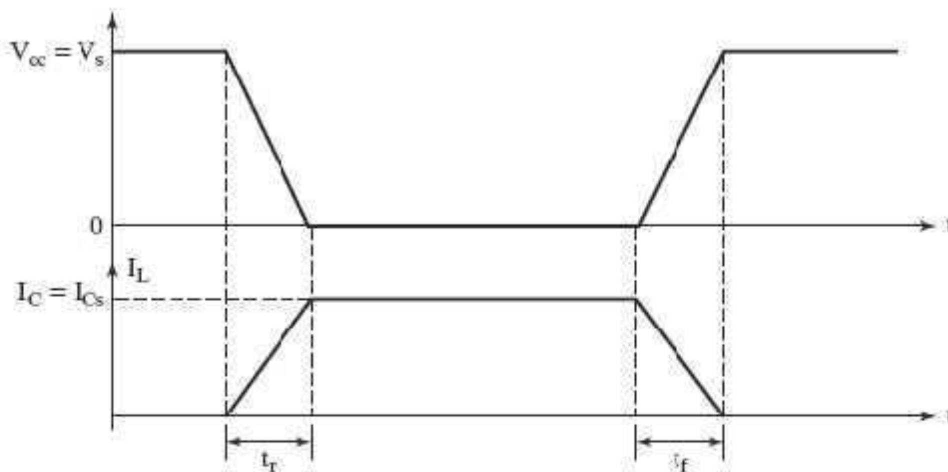


Fig. 11: Dynamic current sharing

BJTs have a negative temperature coefficient. During current sharing, if one BJT carries more current, its on-state resistance decreases and its current increases further, whereas MOSFETS have positive temperature coefficient and parallel operation is relatively easy. The MOSFET that initially draws higher current heats up faster and its on-state resistance increases, resulting in current shifting to the other devices. IGBTs require special care to match the characteristics due to the variations of the temperature coefficients with the collector current.

di/dt AND dv/dt LIMITATIONS

Transistors require certain turn-on and turn-off times. Neglecting the delay time t_d and the storage time t_s, the typical voltage and current waveforms of a BJT switch is shown below.

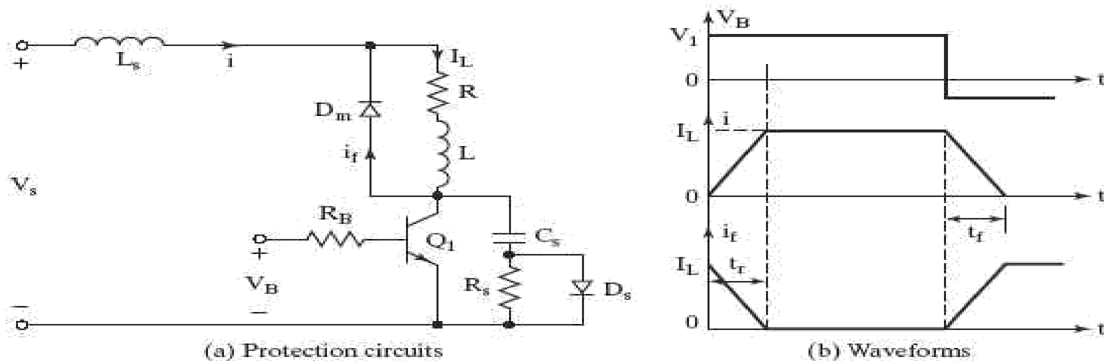


During turn-on, the collector rise and the di/dt is

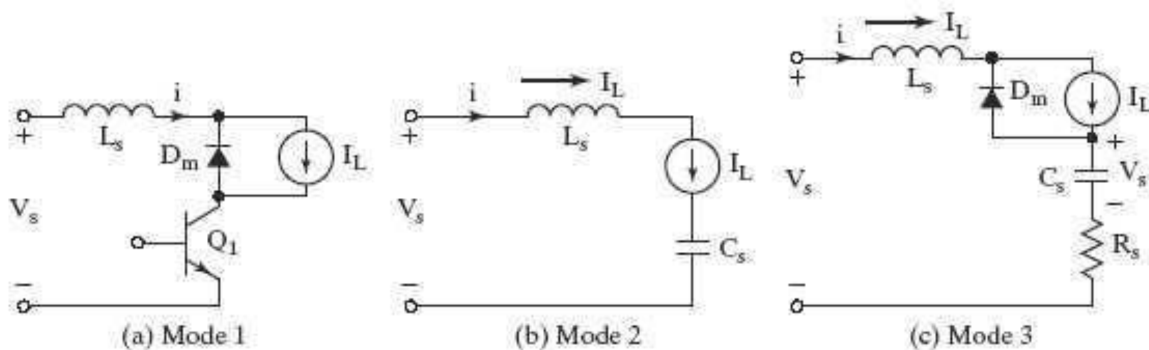
During turn off, the collector emitter voltage must rise in relation to the fall of the collector current, and is

The conditions di/dt and dv/dt in equation (1) and (2) are set by the transistor switching characteristics and must be satisfied during turn on and turn off. Protection circuits are normally required to keep the operating di/dt and dv/dt within the allowable *limits of transistor. A typical switch with di /dt* and *dv /dt* protection is shown in figure *(a), with operating wave forms in figure (b). The RC network across the transistor is known as the snubber circuit or snubber and limits the dv/dt* . The inductor L_S , which *limits the di/dt* , is sometimes called series snubber.

Let us assume that under steady state conditions the load current I_L is free wheeling through diode D_m, which has negligible reverse reco`very time. When transistor Q_1 is turned on, the collector current rises and current of diode D_m falls, because D_m will behave as short circuited. The equivalent circuit during turn on is shown in figure below

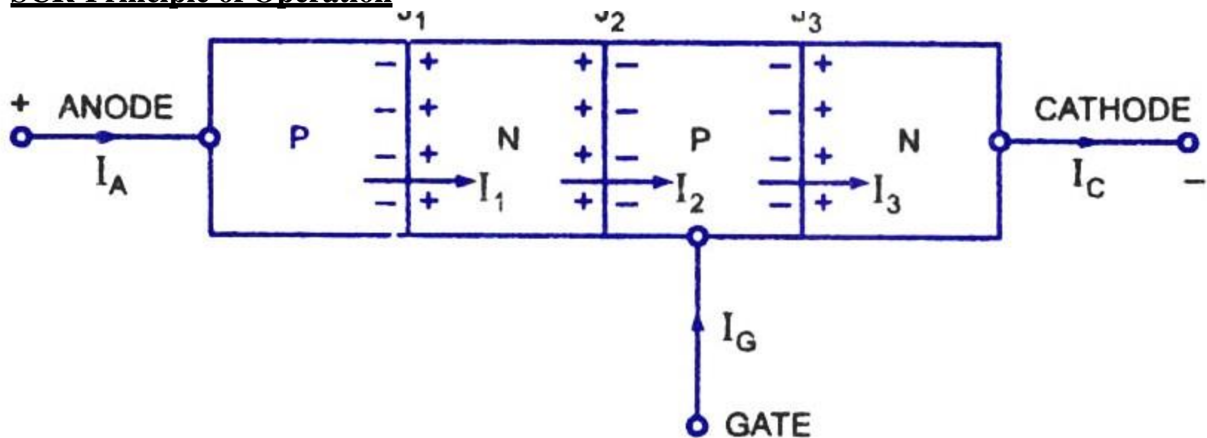


(a) Protection circuits (b) Waveforms



(a) Mode 1 (b) Mode 2 (c) Mode 3

SCR-Principle of Operation



Diagrammatic Representation Showing Current Flow and Voltage Bias in An SCR

The **SCR** is a four-layer, three-junction and a three-terminal device and is shown in fig.a. The end P-region is the anode, the end N-region is the cathode and the inner P-region is the gate. The anode to cathode is connected in series with the load circuit. Essentially the device is a switch. Ideally it remains off (voltage blocking state), or appears to have an infinite impedance until both the anode and gate terminals have suitable positive voltages with respect to the cathode terminal.

The thyristor then switches on and current flows and continues to conduct without further gate signals. Ideally the thyristor has zero impedance in conduction state. For switching off or reverting to the blocking state, there must be no gate signal and the anode current must be reduced to zero. Current can flow only in one direction.

In absence of external bias voltages, the majority carrier in each layer diffuses until there is a built-in voltage that retards further diffusion. Some majority carriers have enough energy to cross the barrier caused by the retarding electric field at each junction. These carriers then become minority carriers and can recombine with majority carriers. Minority carriers in each layer can be accelerated across each junction by the fixed field, but because of absence of external circuit in this case the sum of majority and minority carrier currents must be zero.

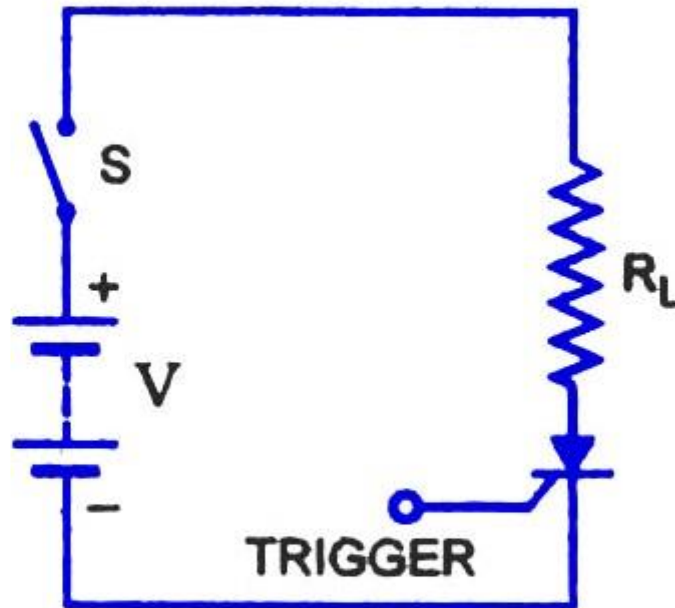
A voltage bias, as shown in figure, and an external circuit to carry current allow internal currents which include the following terms:

The current I_x is due to

- Majority carriers (holes) crossing junction J_1
- Minority carriers crossing junction J_1
- Holes injected at junction J_2 diffusing through the N-region and crossing junction J_1 and
- Minority carriers from junction J_2 diffusing through the N-region and crossing junction J_1.

Similarly I_2 is due to six terms and I_3 is due to four terms.

Turning-off Methods of an SCR



As already mentioned in previous blog post, once the **SCR is fired**, it remains on even when triggering pulse is removed. This ability of the SCR to remain on even when gate current is removed is referred to as latching. So SCR cannot be turned off by simply removing the gate pulse.

There are three methods of switching off the **SCR, namely** natural commutation, reverse bias turn-off, and gate turn-off.

a) Natural Commutation

When the anode current is reduced below the level of the holding current, the SCR turns off. However, it must be noted that rated anode current is usually larger than 1,000 times the holding value. Since the anode voltage remains positive with respect to the cathode in a dc circuit, the anode current can only be reduced by opening the line switch S, increasing the load impedance R_L or shunting part of the load current through a circuit parallel to the SCR, i.e. short-circuiting the device.

(b) Reverse-bias Turn-off

A reverse anode to cathode voltage (the cathode is positive with respect to the anode) will tend to interrupt the anode current. The voltage reverses every half cycle in an ac circuit, so that an SCR in the line would be reverse biased every negative cycle and would turn off. This is called phase commutation or ac line commutation. To create a reverse biased voltage across the SCR, which is in the line of a dc circuit, capacitors can be used. The method of discharging a capacitor in parallel with an SCR to turn-off the SCR is called forced commutation.

In power electronic applications one advantage of using SCRs is that they are compact. The control equipment is also compact if integrated circuits are used. There has also been an attempt to miniaturize capacitors used for forced commutation and for filtering. The former use is important because the currents can be high and thermal dissipation takes high priority in design

considerations. Small sizes of capacitors are at present being achieved by the use of metalized plastic film or a plastic film and aluminium foil.

(c) Gate Turn Off

In some specially designed SCRs the characteristics are such that a negative gate current increases the holding current so that it exceeds the load current and the device turns-off. The current ratings are presently below 10 A and this type will not be considered further.

Firing and Commutation Circuits of SCR

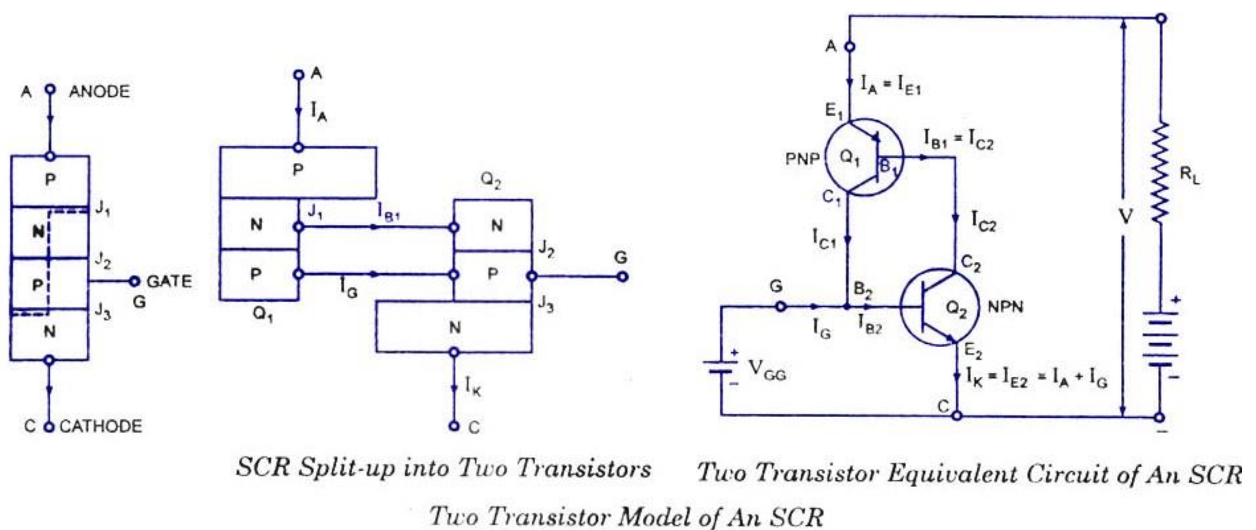
Two Transistor analogy of SCR

The principle of thyristor operation can be explained with the use of its two-transistor model (or two-transistor analogy). Fig. 4.15 (a) shows schematic diagram of a thyristor. From this figure, two-transistor model is obtained by bisecting the two middle layers, along the dotted line, in two separate halves as shown in Fig. 4.15 (b). In this figure, junctions J1 – j2and J2 -J3 can be considered to constitute pnp and npn transistors separately. The circuit representation of the two-transistor model of a thyristor is shown in Fig. 4.15 (c).

In the off-state of a transistor, collector current Ic is related to emitter current IE

as $I_C = \alpha I_E + I_{CBO}$

where α is the common-base current gain and I_{CB0} is the common-base leakage current of collector-base junction of a transistor.



SCR Split-up into Two Transistors *Two Transistor Equivalent Circuit of An SCR*

Two Transistor Model of An SCR

For transistor Q_1 in Fig. 4.15 (c), emitter current I_E = anode current I_a and I_C = collector current I_{C1}. Therefore, for Q_1

$I_{C1} = \alpha_1 I_a + I_{CBO1}$ ……..(4.3)

where α_1 = common-base current gain of Q_1

and I_{CBO1} = common-base leakage current of Q_1

Similarly, for transistor Q_2, the collector current I_{C2} is given

by $I_{C2} = \alpha_2 \ I_k + \ I_{CBO2}$ …(4.4)

where α_2 – common-base current gain of Q_2,I_{CBO2} =common-base leakage current of Q_2 and

I_k = emitter current of Q_2.

The sum of two collector currents given by Eqs. (4.3) and (4.4) is equal to the external circuit current I_α entering at anode terminal A.

There fore $I_a = I_{C1} + I_{C2}$

$I_a = \alpha_1 \ I_a + I_{CBO1} + \alpha_2 I_k + \ I_{CBO2}$ …(4.5)

When gate current is applied, then $I_k = I_a + I_g$. Substituting this value of I_k in Eq. (4.5) gives

$I_a = \alpha_1 \ I_a + I_{CBO1} + \ \alpha_2 \ (I_a \ + I_g\ ) + I_{CBO2}$

or

$I_a = \alpha_2 \ I_g + I_{CBO1} + I_{CBO2} /[1-(\alpha_1 + \alpha_2)]$

For a silicon transistor, current gain α is very low at low emitter current. With an increase in emitter current, a builds up rapidly as shown in Fig. 4.16. With gate current I_g = 0 and with thyristor forward biased,($\alpha_1 + \alpha_2$)is very low as per Eq (4.6) and forward leakage current somewhat more than $I_{CBO1} + I_{CBO2}$ flows. If, by some means, the emitter current of two component transistors can be increased so that $\alpha_1 + \alpha_2$ approaches unity, then as per Eq. (4.6) I_a would tend to become infinity thereby turning-on the device. Actually, external load limits the anode current to a safe value after the thyristor begins conduction. The methods of turning-on a thyristor, in fact, are the methods of making $\alpha_1 + \alpha_2$ to approach unity. These 0.25 various mechanisms for turning-on a thyristor are now discussed below :

(i) **GATE Triggering** : With anode positive with respect to cathode and with gate current I_g = 0, Eq. (4.6) shows that anode current, equal to the forward leakage current, is somewhat more than $I_{CBO1} + I_{CBO2}$,Under these conditions, the device is in the forward blocking state.

Now a sufficient gate-drive current between gate and cathode of the transistor is applied. This gate-drive current is equal to base current $I_{B2} = I_g$ and emitter current I_k of transistor Q_2. With the establishment of emitter current I_k of Q_2, current gain α_2 of Q_2 increases and base current I_{B2} causes the existence of collector current $I_{C2} = \beta_2 I_{B2} = \beta_2 \ I_g$. This amplified current I_{C2} serves as the base current I_{B1} of transistor Q_1 With the flow of I_{B1} collector current $I_{C1} = \beta_1 I_{B1} = \beta_1 \beta_2 I_g$ of Q_1comes into existence. Currents I_{B1} and I_{C1} lead to the establishment of emitter current I_a of Q_1 and this causes current gain α_1 to rise as desired. Now current $I_g + I_{CI} = (1 + \beta_1 \beta_2) I_g$ acts as the base current of Q_2 and therefore its emitter current $I_k = I_{CI} + I_g$ With the rise in emitter current I_k α_2 of Q_2 increases and this further causes $I_{C2} = P_2 (1 + \beta_1 \beta_2) I_g$ to rise. As amplified collector current I_{C2} is equal to the base current of Q_1 current gain α_1 eventually rises further. There is thus established a regenerative action internal to the device. This regenerative or positive feedback effect causes $\alpha_1 + \alpha_2$to grow towards unity. As a consequence, anode current begins to grow towards a larger value limited only by load impedance external to the device. When regeneration has grown sufficiently, gate current can be withdrawn. Even after $I_g$is removed, regeneration continues. This characteristic of the thyristor makes it suitable for pulse triggering. Note that thyristor is a latching device

After thyristor is turned on, all the four layers are filled with carriers and all junctions are forward biased. Under these conditions, thyristor has very low impedance and is in the forward on-state.

(ii) **Forward-voltage triggering** : If the forward anode to cathode voltage is increased, the collector to emitter voltages of both the transistors are also increased. As a result, the leakage current at the middle junction J_2 of thyristor increases, which is also the collector current of Q_2 as well as Q_1 With increase in collector currents I_{C1} and I_{C2} due to avalanche effect, the emitter currents of the two transistors also increase causing $\alpha_1 + \alpha_2$ to approach unity. This leads to switching action of the device due to regenerative action. The forward-voltage triggering for turning-on a thyristor may be destructive and should therefore be avoided.

(iii) **dv/dt triggering** : The reversed biased junction J_2 behaves like a capacitor because of the space-charge present there. Let the capacitance of this junction be Cj. For any capacitor, i = C dv/dt.In case it is assumed that entire forward voltage v_a appears across reverse biased junction J_2 then charging current across the junction is given by

$i = C_j \, dv_a / dt$

This charging or displacement current across junction J_2 is collector currents of Q_2 and Q_1 Currents I_{C2}, I_{C1} will induce emitter current in Q_2, Q_1 In case rate of rise of anode voltage is large, the emitter currents will be large and as a result, $\alpha_1 + \alpha_2$ will approach unity leading to eventual switching action of the thyristor.

(iid **Temperature triggering** : At high temperature, the forward leakage current across junction J_2 rises. This leakage current serves as the collector junction current of the component transistors Q_1 and Q_2. Therefore, an increase in leakage current I_{CI}, I_{C2} leads to an increase in the emitter currents of Q_1 Q_2. As a result, $(\alpha_1 + \alpha_2)$ approaches unity. Consequently, switching action of thyristor takes place.

(v) **Light triggering** : When light is thrown on silicon, the electron-hole pairs increase. In the forward-biased thyristor, leakage current across J_2 increases which eventually increases $\alpha_1 + \alpha_2$ to unity as explained before and switching action of thyristor occurs.

As stated before, gate-triggering is the most common method for turning-on a thyristor. Light-triggered thyristors are used in HVDC applications.

The operational differences between thyristor-family and transistor family of devices may now be summarised as under :

i) Once a thyristor is turned on by a gate signal, it remains latched in on-state due to internal regenerative action. However, a transistor must be given a continuous base signal to remain in on-state.

ii) In order to turn-off a thyristor, a reverse voltage must be applied across its anode-cathode terminals. However, a transistor turns off when its base signal is removed.

Different Firing Circuits of SCR:

One common application of the uni junction transistor is the triggering of the other devices such as the SCR, triac etc. The basic elements of such a triggering circuit are shown in figure. The resistor R_E is chosen so that the load line determined by R_E passes through the device characteristic in the negative resistance region, that is, to the right of the peak point but to the left of the valley point, as shown in figure. If the load line does not pass to the right of the peak point P, the device cannot turn on.

For ensuring turn-on of UJT

$R_E < \quad V_{BB} - V_p / I_P$

This can be established as below

Consider the peak point at which $I_{RE} = I_p$ and $V_E = V_P$

(the equality $I_{RE} = I_P$ is valid because the charging current of capacitor, at this instant is zero, that is, the capacitor, at this particular instant, is changing from a charging state to

a discharging state). Then $V_E = V_{BB} - I_{RE} R_E$

So, $R_{E(MAX)} = V_{BB} - V_E / I_{RE} = V_{BB} - V_p / I_P$ *at the peak point.*

At the valley point, V

$I_E = I_V$ and $V_E = V_V$ so that

$V_E = V_{BB} - I_{RE} R_E$

So $R_{E(MIN)} = V_{BB} - V_E / I_{RE} = V_{BB} - V_V / I_V$ or for ensuring turn-off.

$R_E >= V_{BB} - V_V / I_V$

So, the range of resistor R_E is given as

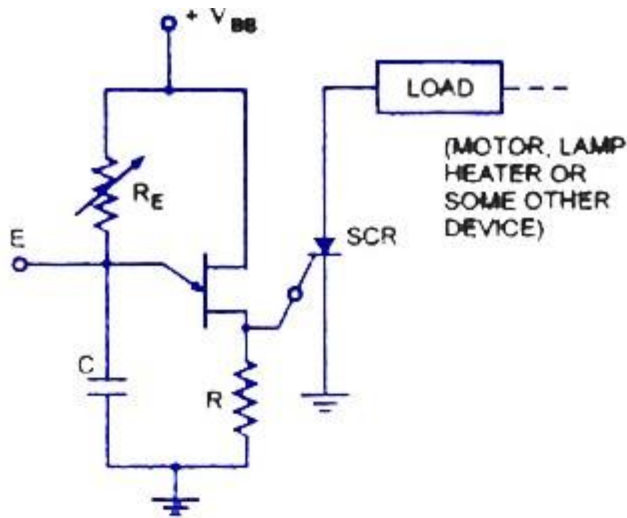
$V_{BB} - V_P / I_P > R_E > V_{BB} - V_V / I_V$

The resistor R is chosen small enough so as to ensure that SCR is not turned on by voltage

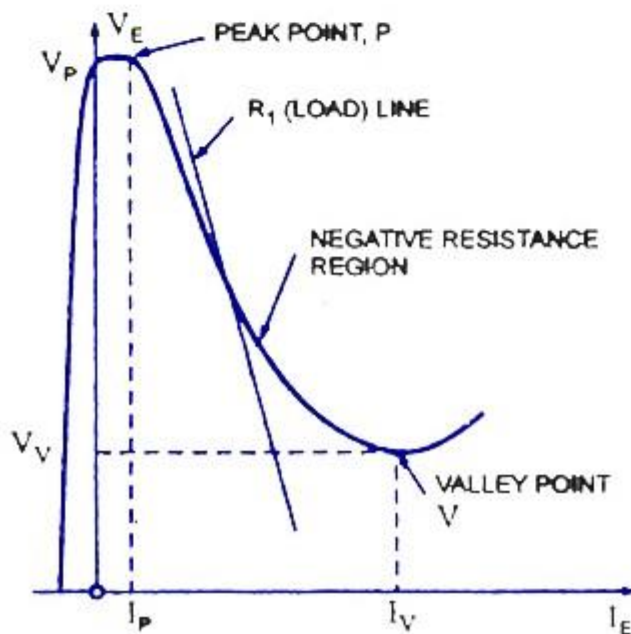
V_R when emitter terminal E is open or $I_E = 0$

The voltage $V_R = RV_{BB}/R + R_{BB}$ for open-emitter terminal.

The capacitor C determines the time interval between triggering pulses and the time duration of each pulse. By varying R_E, we can change the time constant $R_E C$ and alter the point at which the UJT fires. This allows us to control the conduction angle of the SCR, which means the control of load current.



UJT Triggering of An SCR



Series and Parallel connections of SCRs

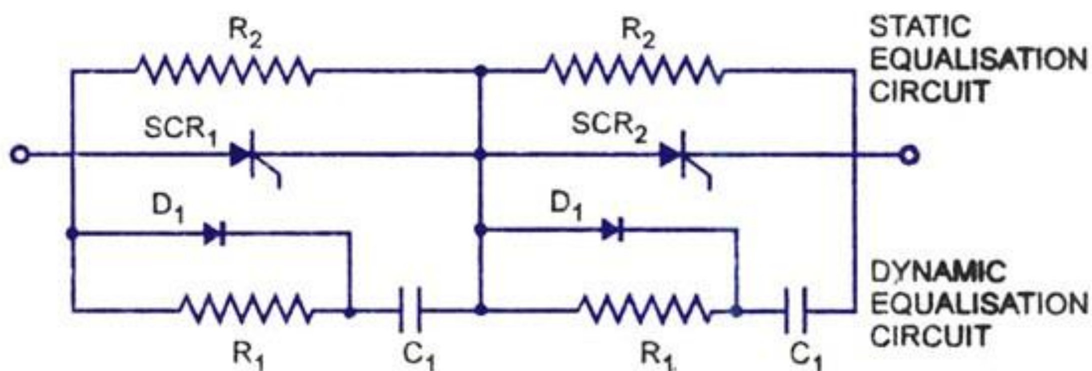
In many power control applications the required **voltage and current ratings** exceed the voltage and current that can be provided by a single SCR. Under such situations the SCRs are required to be connected in series or in parallel to meet the requirements. Sometimes even if the required rating is available, multiple connections are employed for reasons of economy and easy availability of SCRs of lower ratings.

Like any other electrical equipment, characteristics/properties of two SCRs of same make and ratings are never same and this leads to certain problems in the circuit. The mismatching of

SCRs is due to differences in

(i) turn-on time
(ii) turn-off time
(iii) leakage current in forward direction
(iv) leakage current in reverse direction and
(iii) recovery voltage.

Series Connection of an SCR



Equalisation For Series Connection

When the required voltage rating exceeds the SCR voltage rating, a number of SCRs are required to be connected in series to share the forward and reverse voltage. As it is not possible to have SCRs of completely identical characteristics, deviation in characteristics lead to the following two major problems during series connections of the SCRs:

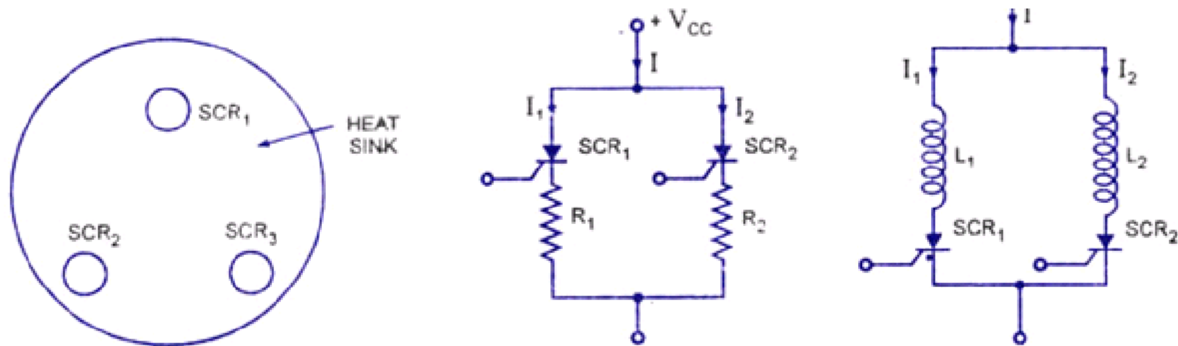
***(i)* Unequal distribution of voltage across SCRs.**

***(ii)* Difference in recovery characteristics.**

Care must be taken to share the voltage equally. For steady-state conditions, voltage sharing is achieved by using a resistance or a Zener diode in parallel with each SCR. For transient voltage sharing a low non-inductive resistor and capacitor in series are placed across each SCR, as shown in figure. Diodes D_1 connected in parallel with resistor R_l, helps in dynamic stabilisation. This circuit reduces differences between blocking voltages of the two devices within permissible limits. Additionally the R-C circuit can also serve the function of**'snubber circuit'**. Values of R_1 and C_1 can primarily be calculated for snubber circuit and a check can be made for equalization. If ΔQ is the difference in recovery charge of two devices arising out of different recovery current for different time and ΔV is the permissible difference in blocking voltage then $C_1 = \Delta Q / \Delta V$.

The value of resistance R_x should be sufficient to over damp the circuit.
Since the capacitor C_1 can discharge through the SCR during turn-on, there can be excessive power dissipation, but the switching current from C_1 is limited by the resistor R_1 This resistance also serves the purpose of damping out ‘ringing’ which is oscillation of C_1 with the circuit inductance during commutation. All the SCRs connected in series should be turned-on at the same time when signals are applied to their gates simultaneously.

Parallel Connection of an SCR



When the load current exceeds the SCR current rating, SCRs are connected in parallel to share the load current. But when SCRs are operated in parallel, the current sharing between them may not be proper. The device having lower dynamic resistance will tend to share more current. This will raise the temperature of that particular device in comparison to other, thereby reducing further its dynamic resistance and increasing current through it. This process is cumulative and continues till the device gets punctured.
Some other factors which directly or indirectly add to this problem are difference in turn-on time, delay time, finger voltage* and loop inductance. Arrangement of SCRs in the cubicle also plays vital role. When the SCRs are connected in parallel, it must be ensured that the latching current level of the all the SCRs is such that when gate pulse is applied, all of them turn-on and remain on when the gate pulse is removed. Further the holding currents of the devices should not be so much different that at reduced load current one of the device gets turned-off because of fall of current through it blow its holding current value. This is particularly important because on increase in load current, the device which has stopped conducting cannot start in the absence of gate pulse.
Another point to be considered is the on-state voltage across the device. For equal sharing of currents by the devices voltage drop across the parallel paths must be equal. For operation of all the SCRs connected in parallel at the same temperature, it becomes necessary to use a common heat sink for their mounting, as illustrated in figure. Resistance compensation used for dc circuits is shown in figure. In this circuit the resistors R_x and R_2 are chosen so as to cause equal voltage drop in both arms. Inductive compensation used for ac circuits is shown in figure The difference in characteristics due to different turn-on time, delay time, finger voltage, latching current,

holding current can be minimized by using inductive compensation. Firing circuits giving high rate of rise can be used to reduce mismatch of gate characteristics and delay time.

Current sharing circuits must be designed so as to distribute current equally at maximum temperature and maximum anode current. This is done to ensure that the devices share current equally under worst operating conditions. Mechanical arrangement of SCRs also plays an important role in reducing mismatching. Cylindrical construction is perhaps the best from this point of view.

Derating. Even with all the measures taken, it is preferable to derate the device for series/parallel operation. Another reason for derating is poor cooling and heat dissipation as number of devices operate in the same branch of the circuit.

Normal derating factors are 10 to 15% for parallel connection of SCRs depending upon the number of devices connected in parallel. Higher voltage safety factor is taken when SCRs are connected in series.

Commutation circuits

- Requirements to be satisfied for the successful turn-off of a SCR
- The turn-off groups as per the General Electric classification
- The operation of the turn-off circuits
- Design of a SCR commutation circuit

A thyristor can be turned ON by applying a positive voltage of about a volt or a current of a few tens of milliamps at the gate-cathode terminals. However, the amplifying gain of this regenerative device being in the order of the 10^8, the SCR cannot be turned OFF via the gate terminal. It will turn-off only after the anode current is annulled either naturally or using forced commutation techniques. These methods of turn-off do not refer to those cases where the anode current is gradually reduced below Holding Current level manually or through a slow process. Once the SCR is turned ON, it remains ON even after removal of the gate signal, as long as a minimum current, the Holding Current, I_h, is maintained in the main or rectifier circuit.

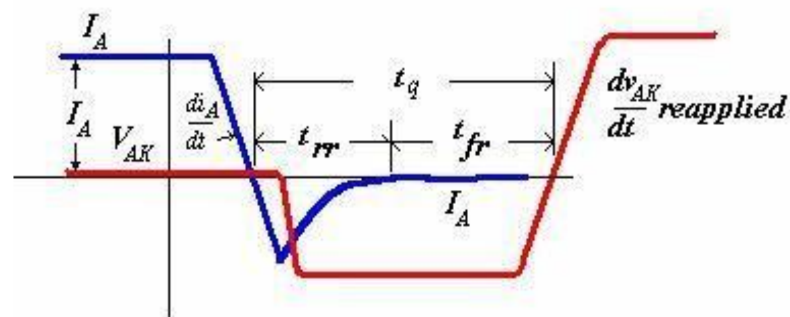


Fig. 3.1 Turn-off dynamics of the SCR

In all practical cases, a negative current flows through the device. This current returns to zero only after the reverse recovery time t_{rr}, when the SCR is said to have regained its reverse blocking capability. The device can block a forward voltage only after a further t_{fr}, the forward recovery time has elapsed. Consequently, the SCR must continue to be reverse-biased for a minimum of $t_{fr} + t_{rr} = t_q$, the rated turn- off time of the device. The external circuit must therefore

reverse bias the SCR for a time $t_{off} > t_q$. Subsequently, the reapplied forward biasing voltage must rise at a dv/dt < dv/dt (reapplied) rated. This dv/dt is less than the static counterpart. General Electric has suggested six classification methods for the turn-off techniques generally adopted for the SCR. Others have chosen different classification rules.

SCRs have turn-off times rated between 8 - 50 μsecs. The faster ones are popularly known as 'Inverter grade' and the slower ones as 'Converter grade' SCRs. The latter are available at higher current levels while the faster ones are expectedly costlier.

Classification of forced commutation methods

The six distinct classes by which the SCR can be turned off are:

Class A Self commutated by a resonating load
Class B Self commutated by an L-C circuit
Class C C or L-C switched by another load carrying SCR
Class D C or L-C switched by an auxiliary SCR

Class E An external pulse source for commutation Class
F AC line commutation

These examples show the classes as choppers. The commutation classes may be used in practice in configurations other than choppers.

Class A, Self commutated by resonating the load

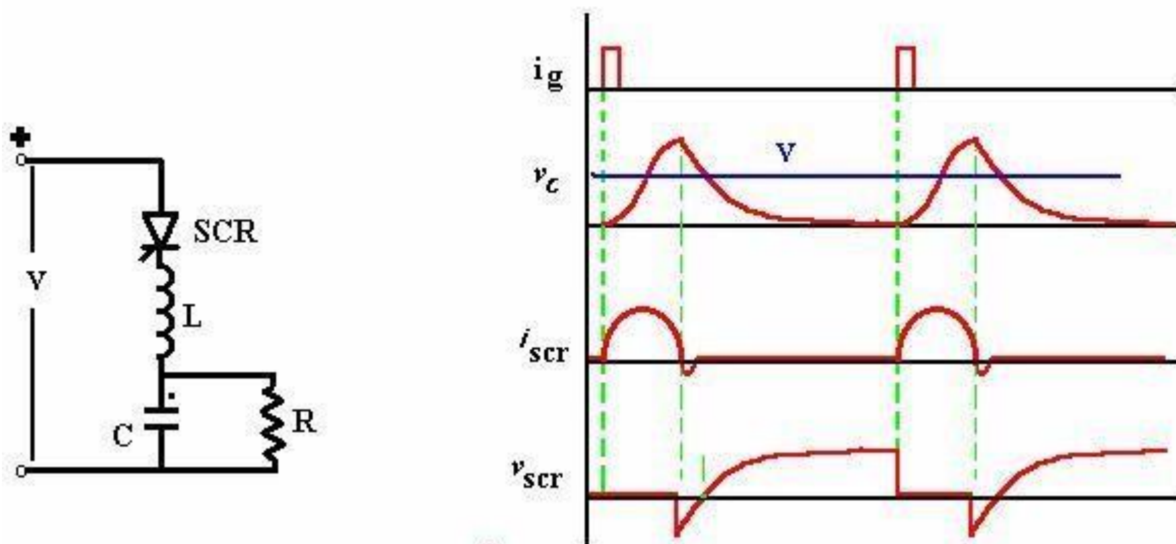


Fig. 3.2 A resonant load commutated SCR and the corresponding waveforms

When the SCR is triggered, anode current flows and charges up C with the dot as positive. The L-C-R form a second order under-damped circuit. The current through the SCR builds up and completes a half cycle. The inductor current will then attempt to flow through the SCR in the reverse direction and the SCR will be turned off.

The capacitor voltage is at its peak when the SCR turns off and the capacitor discharges into the resistance in an exponential manner. The SCR is reverse-biased till the capacitor voltages returns to the level of the supply voltage V.

Class B, Self commutated by an L-C circuit

The Capacitor C charges up in the dot as positive before a gate pulse is applied to the SCR. When SCR is triggered, the resulting current has two components.

The constant load current I_{load} flows through R - L load. This is ensured by the large reactance in series with the load and the freewheeling diode clamping it. A sinusoidal current flows through the resonant L- C circuit to charge-up C with the dot as negative at the end of the half cycle. This current will then reverse and flow through the SCR in opposition to the load current for a small fraction of the negative swing till the total current through the SCR becomes zero. The SCR will turn off when the resonant–circuit (reverse) current is just greater than the load current.

The SCR is turned off if the SCR remains reversed biased for $t_q > t_{off}$, and the rate of rise of the reapplied voltage < the rated value.

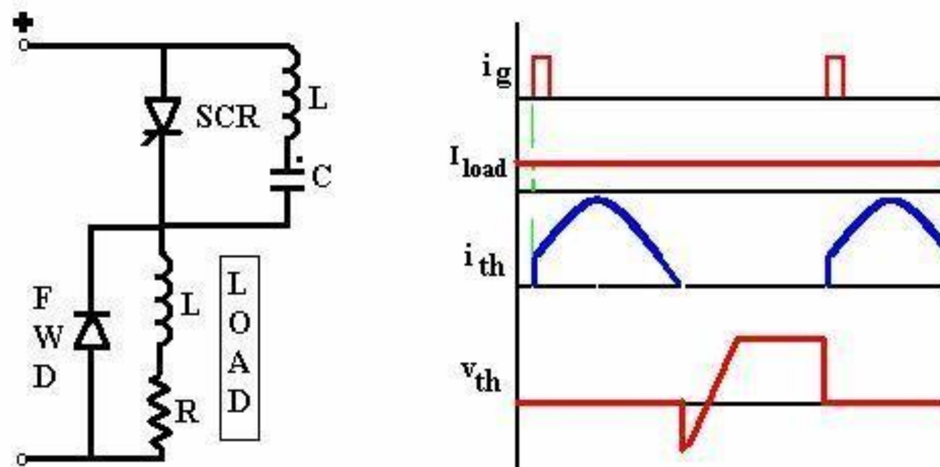


Fig. 3.3 Class B, L-C turn-off

Problem #1

A Class B turn-off circuit commutates an SCR. The load current is constant at 10 Amps. Dimension the commutating components L and C. The supply voltage is 100VDC.

Soln # 1

The commutating capacitor is charged to the supply voltage = 100 V

The peak resonant current is,

$$i_{peak} = V\sqrt{\frac{C}{L}}$$

Assuming,

$$i_{peak} \simeq 1.5 . I_{load}$$

$$\frac{C}{L} = \left(\frac{15}{100}\right)^2 = 0.0225$$

The SCR commutates when the total current through it reaches zero.This corresponds to 0.73 rads after the zero crossing of the resonant current. The capacitor voltage at that instant is 75 volts. After the SCR turns off, the capacitor is charged linearly by the load current.

If the SCR is to commutate at twice this load current, for a rated "Inverter grade' SCR turn-off time of 20 μsecs,

It can be observed that if the peak of the commutating current is just equal to the load current, the turn-off time would be zero as the capacitor would not be able to impress any negative voltage on the SCR.

Class C, C or L-C switched by another load–carrying SCR

This configuration has two SCRs. One of them may be the main SCR and the other auxiliary. Both may be load current carrying main SCRs. The configuration may have four SCRs with the load across the capacitor, with the integral converter supplied from a current source. Assume SCR_2 is conducting. C then charges up in the polarity shown. When SCR_1 is triggered, C is switched across SCR_2 via SCR_1 and the discharge current of C opposes the flow of load current in SCR_2.

Fig. 3.4 Class C turn-off, SCR switched off by another load-carring SCR

Class D, L-C or C switched by an auxiliary SCR

Example 1

The circuit shown in Figure 3.3 (Class C) can be converted to Class D if the load current is carried by only one of the SCR's, the other acting as an auxiliary turn-off SCR. The auxiliary SCR would have a resistor in its anode lead of say ten times the load resistance.

Fig. 3.5 Class D turn-off. Class D commutation by a C (or LC) switched by an Auxiliary SCR.

Example 2

SCR_A must be triggered first in order to charge the upper terminal of the capacitor as positive. As soon as C is charged to the supply voltage, SCR_A will turn off. If there is substantial inductance in the input lines, the capacitor may charge to voltages in excess of the supply voltage. This extra voltage would discharge through the diode-inductor-load circuit.

When SCR_M is triggered the current flows in two paths: Load current flows through the load and the commutating current flows through C- SCR_M -L-D network. The charge on C is reversed and held at that level by the diode D. When SCR_A is re-triggered, the voltage across C appears across SCR_M via SCR_A and SCR_M is turned off. If the load carries a constant current as in Fig. 3.4, the capacitor again charges linearly to the dot as positive.

Problem # 2

A Class D turn-off circuit has a commutating capacitor of 10 μF. The load consists of a clamped inductive load such that the load current is reasonably constant at 25 amperes. The 'Inverter grade' SCR has a turn-off time of 12 μsecs. Determine whether the SCR will be satisfactorily commutated. Also dimension the commutating inductor. The supply voltage is 220 VDC.

Soln # 2

The capacitor is initially charged to the supply voltage **220 V** at the end of the conduction period of SCR_A.

When SCR_M is triggered, the 25 Amps load current and the L-C ringing current flows through it. Peak current through SCR is

$$i_{peak} = 25 + 220\sqrt{C/L} \quad Amps$$

Selecting L such that $i_{peak} \sim 1.5$. load current,

$$\sqrt{\frac{C}{L}} = \frac{25}{2.220} = 0.0568$$

$$L = 3.1 \quad mH$$

Assuming that the capacitor charges to 70% of its original charge because of losses in the C- SCR_M -L-D network, and it charges linearly when SCR_A is again triggered,

$$I_{load} .t_q = 10(0.7.220)10^{-6} = 1540.10^{-6}$$

$$t_q = 1540 / 25 = 61.6 \ \mu sec$$

The SCR can therefore be successfully commutated.

The maximum current that can be commutated with the given Capacitor at the 220 V supply voltage is

$$I_{load} = 1540 / 12 = 128 \quad Amps$$

For the 25 Amps load current the capacitor just enough would have a rating of

$$C = I_{load} .t_q /(0.7.220) = (25.12) /154 = 1.95 \approx 2.0 \quad \mu F$$

If the supply voltage is reduced by a factor **K**, the required capacitor rating increases by the same factor **K** for the same load current**.**

Class E – External pulse source for commutation

The transformer is designed with sufficient iron and air gap so as not to saturate. It is capable of carrying the load current with a small voltage drop compared with the supply voltage.

When SCR1 is triggered, current flows through the load and pulse transformer. To turn SCR_1 off a positive pulse is applied to the cathode of the SCR from an external pulse generator via the pulse transformer. The capacitor C is only charged to about 1 volt and for the duration of the turn-off pulse it can be considered to have zero impedance. Thus the pulse from the transformer reverses the voltage across the SCR, and it supplies the reverse recovery current and holds the voltage negative for the required turn-off time.

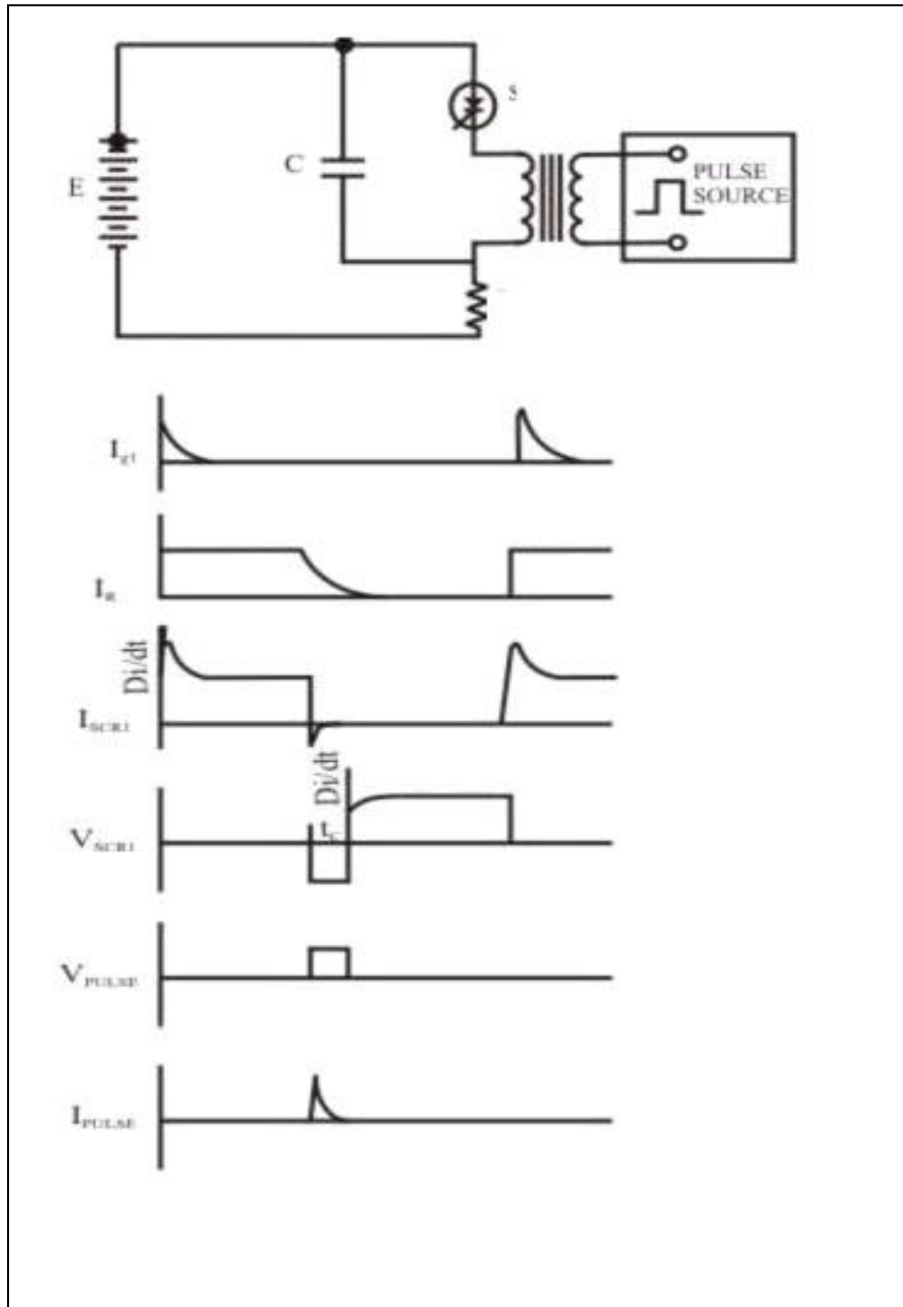


Fig. 3.6 Class E, External pulse commutation

Class F, AC line commutated

If the supply is an alternating voltage, load current will flow during the positive half cycle. With a highly inductive load, the current may remain continuous for some time till the

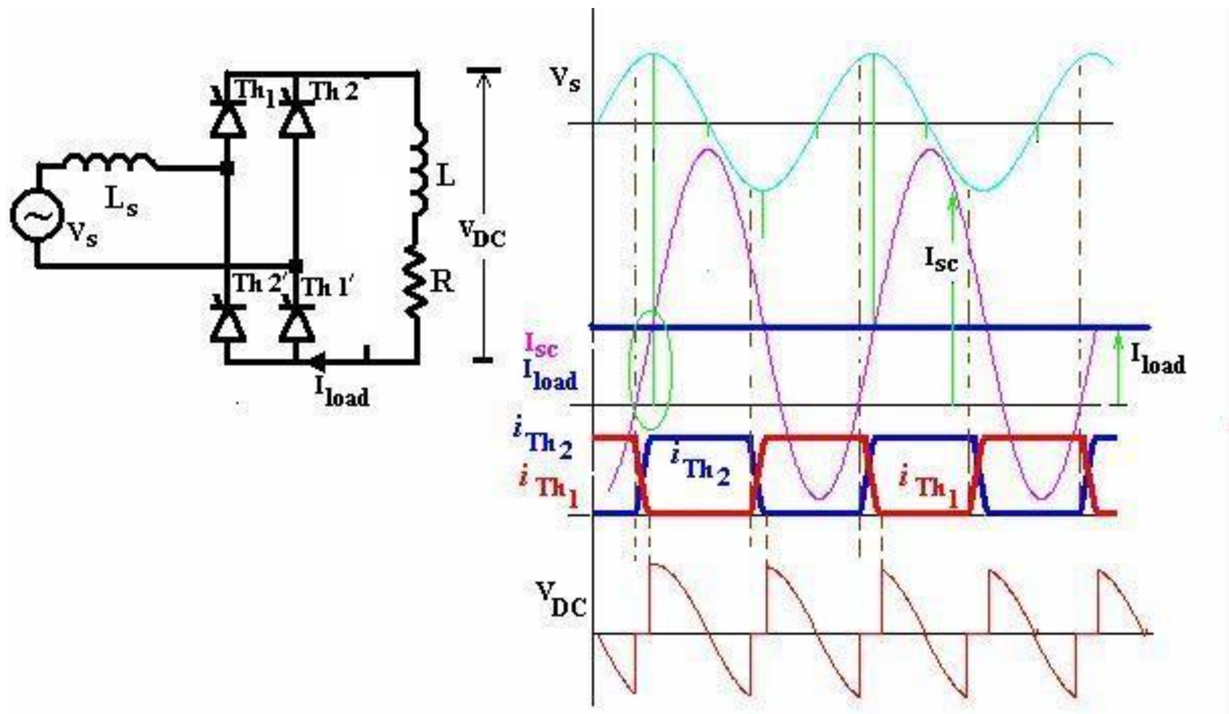


Fig. 3.7 Class F, natural commutation by supply voltage

energy trapped in the load inductance is dissipated. During the negative half cycle, therefore, the SCR will turn off when the load current becomes zero 'naturally'. The negative polarity of the voltage appearing across the outgoing SCR turns it off if the voltage persists for the rated turn-off period of the device. The duration of the half cycle must be definitely longer than the turn-off time of the SCR.

The rectifier in Fig.3.6 is supplied from an single phase AC supply. The commutation process involved here is representative of that in a three phase converter. The converter has an input inductance L_s arising manly out of the leakage reactance of the supply transformer. Initially, SCRs Th_1 and $Th_{1'}$ are considered to be conducting. The triggering angle for the converter is around 60^0. The converter is operating in the continuous conduction mode aided by the highly-inductive load.

When the incoming SCRs, Th_2 and $Th_{2'}$ are triggered, the current through the incoming devices cannot rise instantaneously to the load current level. A circulating current I_{sc} builds up in the short-circuited path including the supply voltage, V_s-L_s-$Th_{1'}$- Th_2 and V_s- L_s-$Th_{2'}$-Th_1 paths. This current can be described by:

$$I_{sc} = \frac{V_s \sin(\omega t - 90^0)}{\omega L_s} + \frac{V_s}{\omega L_s}\cos\alpha = \frac{V_s \cos(\omega t)}{\omega L_s} + \frac{V_s}{\omega L_s}\cos\alpha$$

where α the triggering angle and I_{sc} and V_s as shown in Fig. 3.6.

This expression is obtained with the simplifying assumption that the input inductance contains no resistances. When the current rises in the incoming SCRs, which in the outgoing

ones fall such that the total current remains constant at the load current level. When the current in the incoming ones reach load current level, the turn-off process of the outgoing ones is initiated. The reverse biasing voltage of these SCRs must continue till they reach their forward blocking state. As is evident from the above expression, the overlap period is a function of the triggering angle. It is lowest when $\alpha \sim 90^0$. These SCRs being 'Converter grade', they have a larger turn-off time requirement of about 30-50 μsecs.

The period when both the devices conduct is known as the 'overlap period'. Since all SCRs are in conduction, the output voltage for this period is zero. If the 'fully-controlled' converter in Fig. 3.7 is used as an inverter with triggering angles > 90^0, the converter triggering can be delayed till the 'margin angle' which includes the overlap angle and the turn-off time of the SCR - both dependent on the supply voltages.

Rate of rise of forward voltage, dv/dt

The junctions of any semiconductor exhibit some unavoidable capacitance. A changing voltage impressed on this junction capacitance results in a current, I = C dv/dt. If this current is sufficiently large a regenerative action may occur causing the SCR to switch to the on state. This regenerative action is similar to that which occurs when gate current is injected. The critical rate of rise of off-state voltage is defined as the maximum value of rate of rise of forward voltage which may cause switching from the off-state to the on-state.

Since dv/dt turn-on is non-destructive, this phenomenon creates no problem in applications in which occasional false turn -on does not result in a harmful affect at the load. Heater application is one such case. However, at large currents where dv/dt turn-on is accompanied by partial turn-on of the device area a high di/dt occurs which then may be destructive.

The majority of inverter applications, however, would result in circuit malfunction due to dv/dt turn-on. One solution to this problem is to reduce the dv/dt imposed by the circuit to a value less than the critical dv/dt of the SCR being used. This is accomplished by the use of a circuit similar to those in Figure 3.8 to suppress excessive rate of rise of anode voltage. Z represents load impedance and circuit impedance. Variations of the basic circuit is also shown where the section of the network shown replaces the SCR and the R-C basic snubber.

Since circuit impedances are not usually well defined for a particular application, the values of R and C are often determined by experimental optimization. A technique can be used to simplify snubber circuit design by the use of nomographs which enable the circuit designer to select an optimized R-C snubber for a particular set of circuit operating conditions.

Another solution to the dv/dt turn-on problem is to use an SCR with higher dv/dt turn-on problem is to use an SCR with higher dv/dt capability. This can be done by selecting an SCR designed specially for high dv/dt applications, as indicated by the specification sheet. Emitter shorting is a manufacturing technique used to accomplish high dv/dt capability.